

EG060V-EA

Reference Design

LTE-A Module Series

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Status: Released



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Quectel Wireless Solutions Co., Ltd.

Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China

Tel: +86 21 5108 6236

Email: info@quectel.com

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About the Document

Revision History

Version	Date	Author	Description
-	2020-09-16	King MA/ Benjamin CHAI	Creation of the document
1.0	2020-09-25	King MA/ Benjamin CHAI	First official release

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1 Reference Design

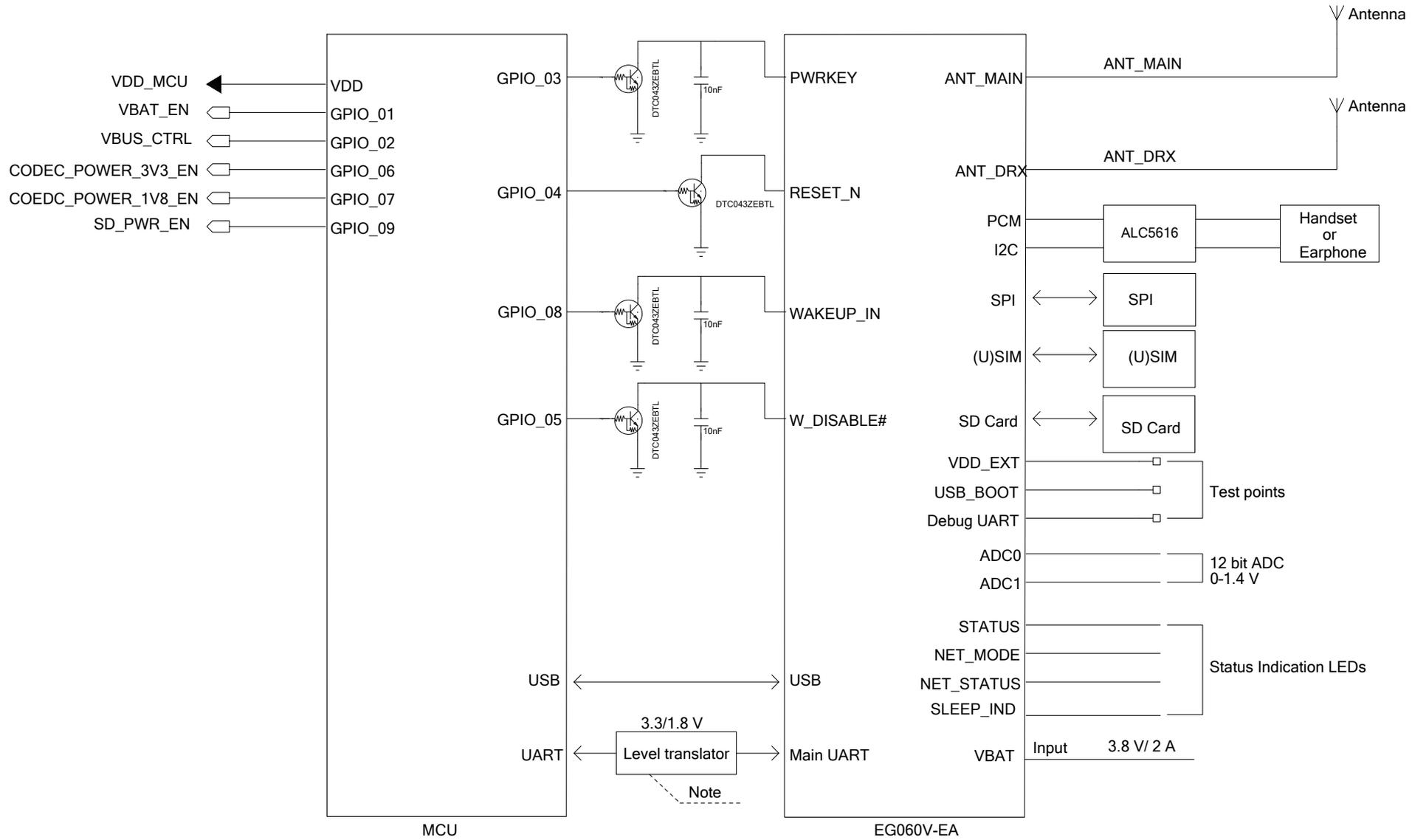
1.1. Introduction

This document provides the reference design for Quectel EG060V-EA module, including the designs of power supply, module interfaces, MCU interfaces, (U)SIM and UART interfaces, Audio Codec and Audio Interface, SD card interface, RF Antenna, SLIC, etc.

1.2. Schematics

The schematics illustrated in the following pages are provided for reference only.

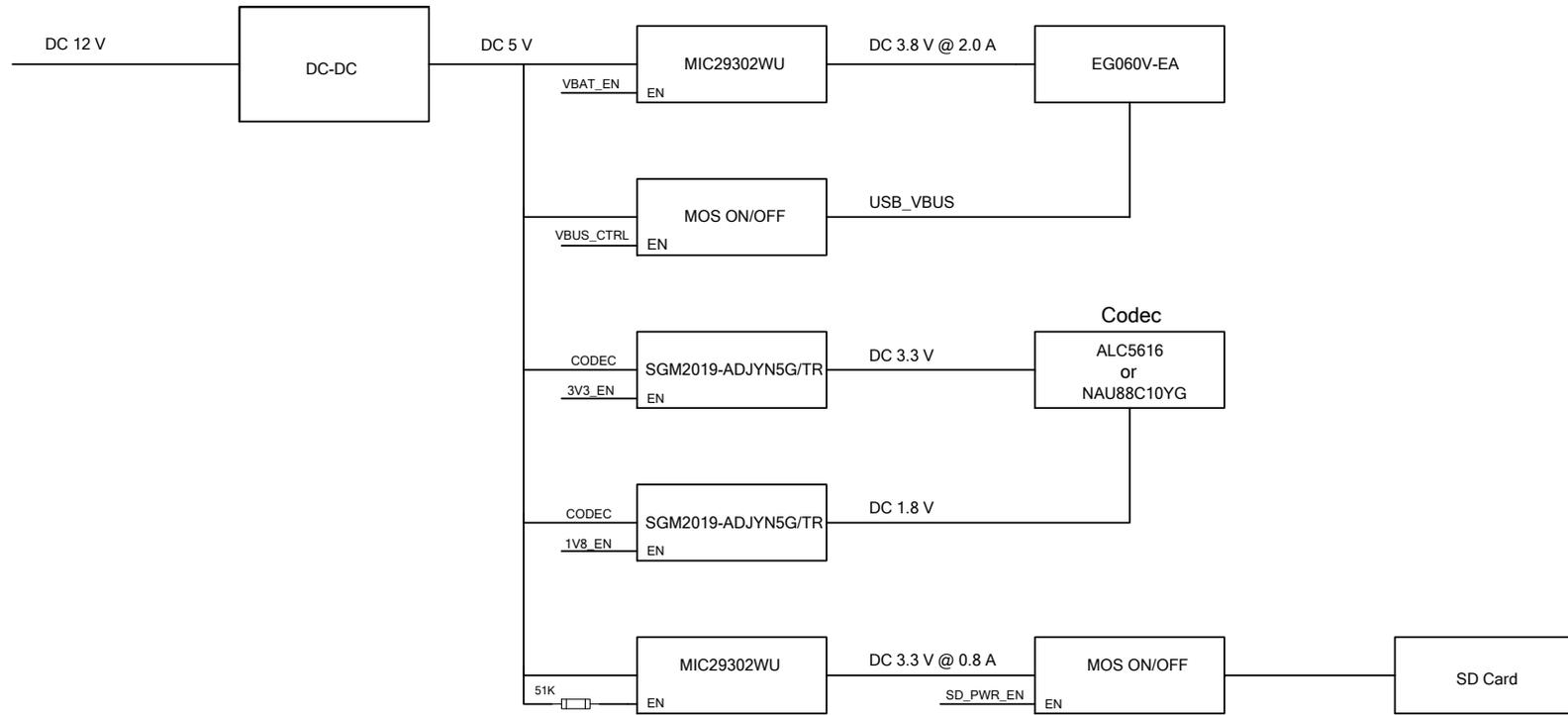
Block Diagram



Note:
A transistor translation circuit or a level translator TXS0108EPWR provided by Texas Instruments (TI) is recommended.

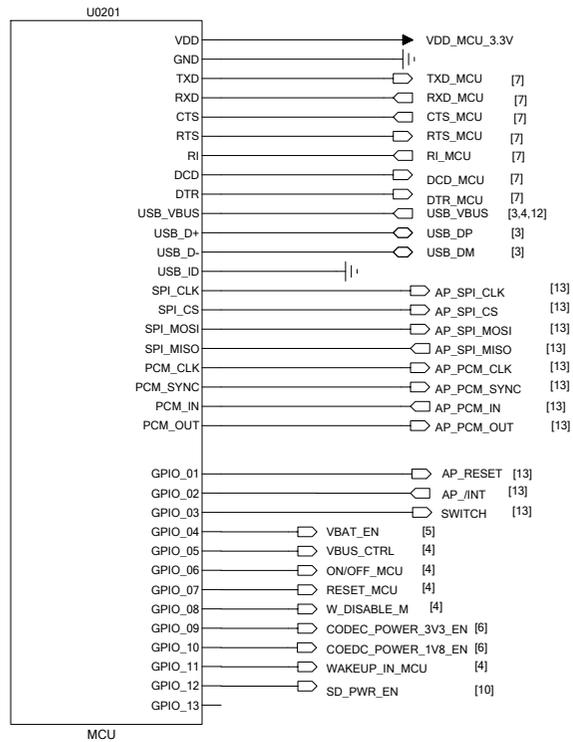
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Power Supply Block Diagram

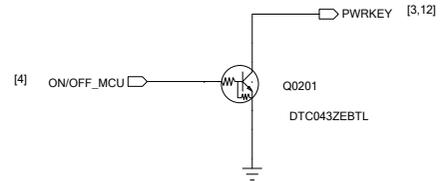


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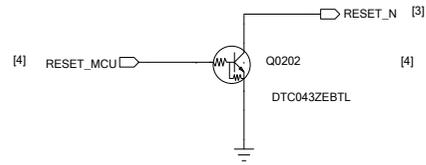
MCU Interfaces



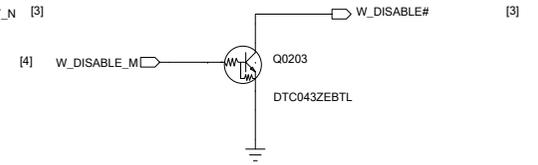
It is used to turn on/off the module.



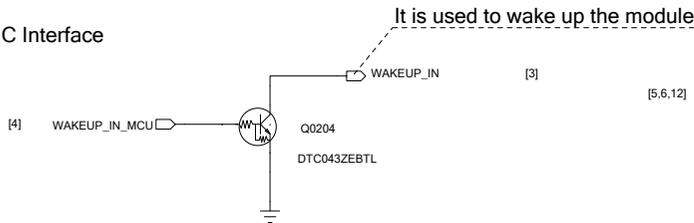
It is used to reset the module.



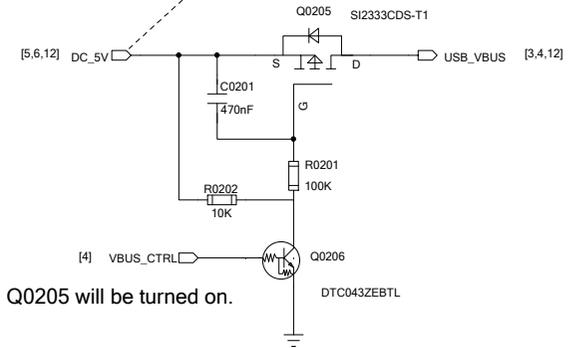
It is used to set the module to airplane mode.



AP: SLIC Interface



5 V power source from the motherboard.



When VBUS_CTRL is at high level, Q0205 will be turned on.

Notes:

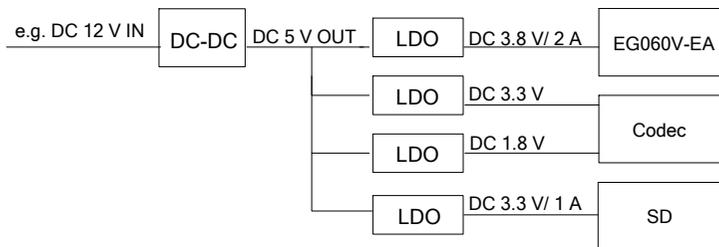
1. U0201 represents your MCU.
2. EG060V-EA can only work as a USB slave device and support USB 2.0. To communicate with the module via USB interface, MCU needs to support USB host or OTG function. The USB_VBUS pins of MCU and the module should be powered by a 5 V power system for USB detection. VBUS_CTRL is used to turn on/off USB_VBUS power supply. When it is at high level, USB_VBUS will be powered on.
3. Transistor circuits (Q0201 to Q0204) are used for level translation.

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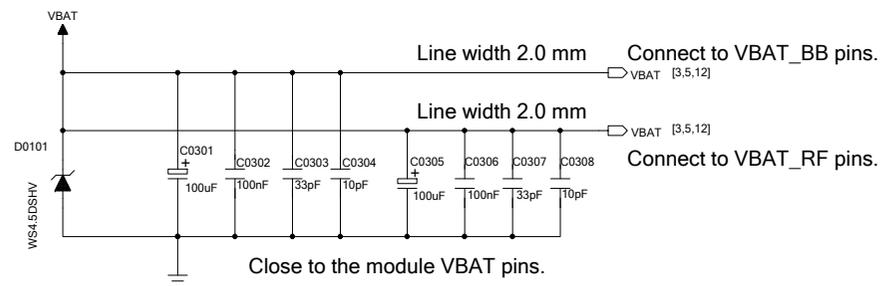
Power Supply Design (Part 1)

DC-DC Application



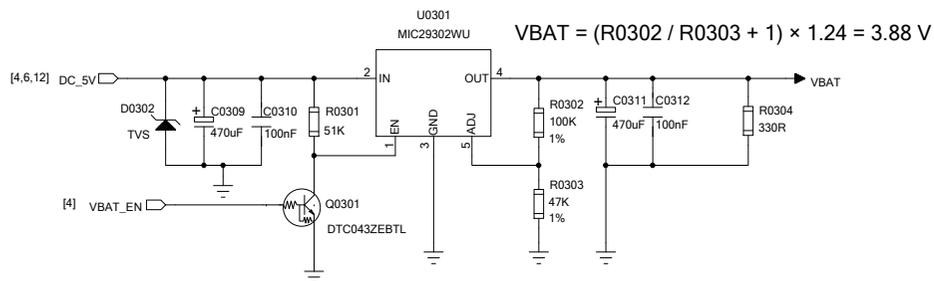
Note:
When the input voltage is above 7 V, a DC-DC converter should be used to convert the high input voltage to 5 V output, and then the LDOs will generate 3.8 V, 3.3 V, and 1.8 V typical voltages respectively.

VBAT Design



- Notes:**
1. The power supply must be able to provide sufficient current (at least 2 A).
 2. VBAT should be routed in star structure to VBAT_BB and VBAT_RF pins.
 3. The recommended operating voltage of VBAT is 3.3-4.3 V.

LDO Application



Note:
The load current of MIC29302WU is recommended to be greater than 10 mA.

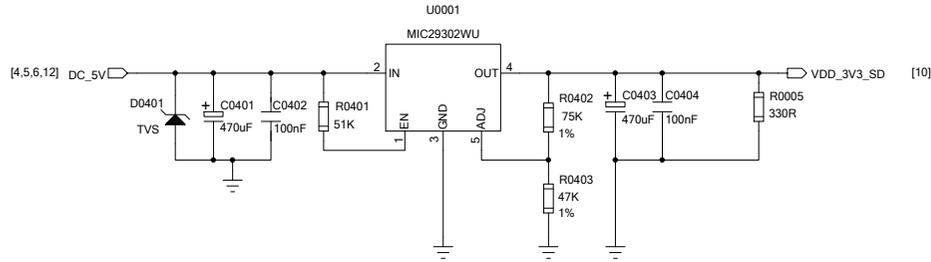
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Power Supply Design (Part 2)

Supply Power to SD Card

$$VDD_3V3_SD = (R0402 / R0403 + 1) \times 1.24 = 3.3 \text{ V}$$

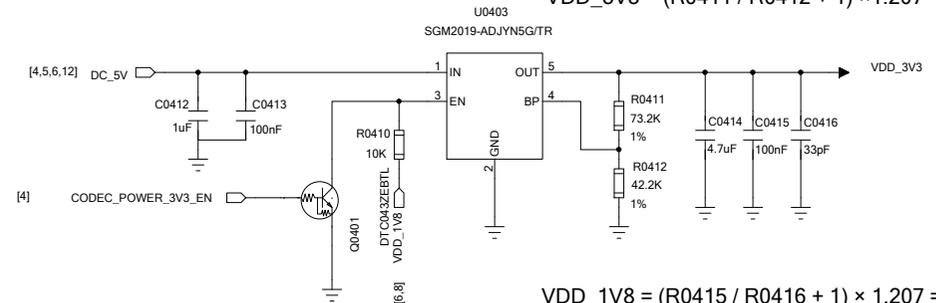


Note:

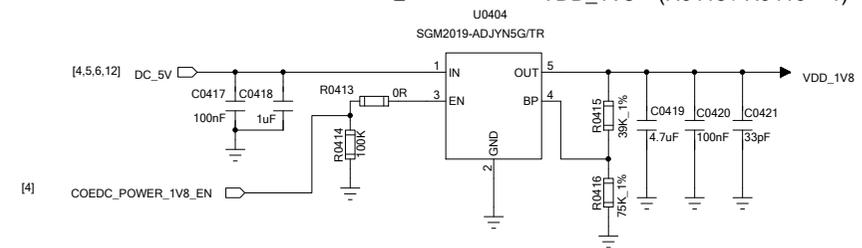
The load current of MIC29302WU is recommended to be greater than 10 mA.

Supply Power to PCM Codec

$$VDD_3V3 = (R0411 / R0412 + 1) \times 1.207 = 3.3 \text{ V}$$



$$VDD_1V8 = (R0415 / R0416 + 1) \times 1.207 = 1.8 \text{ V}$$



Notes:

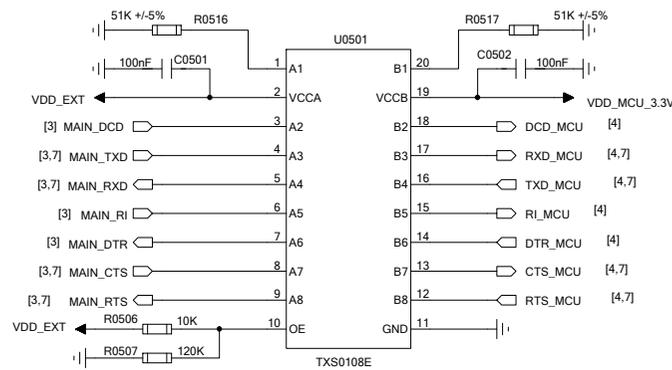
- CODEC_POWER_3V3_EN must be at low level to ensure normal voltage output from VDD_3V3.
If VDD_3V3 power supply needs to be switched off, keep CODEC_POWER_3V3_EN at high level.
- Please follow the power-on and power-off sequences below to ensure that the audio codec works normally.
Power-on Sequence: power on VDD_1V8 first, then VDD_3V3.
Power-off Sequence: power off VDD_3V3 first, then VDD_1V8.

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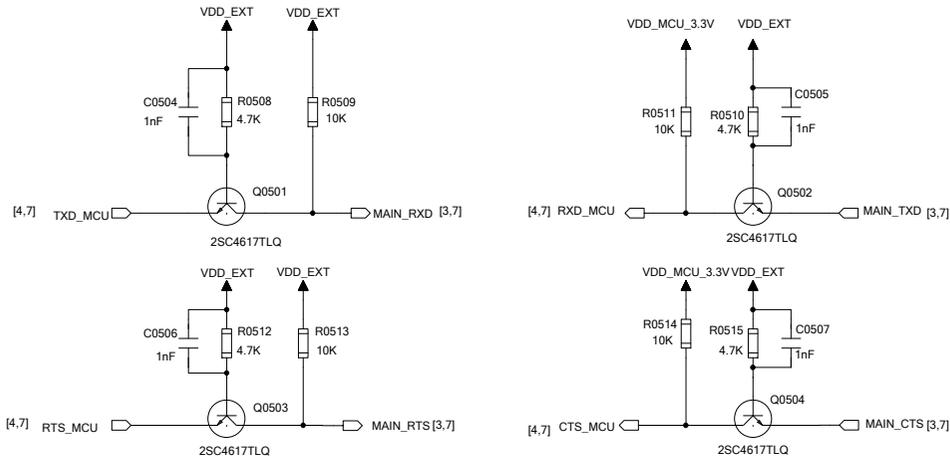
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(U)SIM Interface and UART Design

UART Level Translation - IC Solution (Recommended)



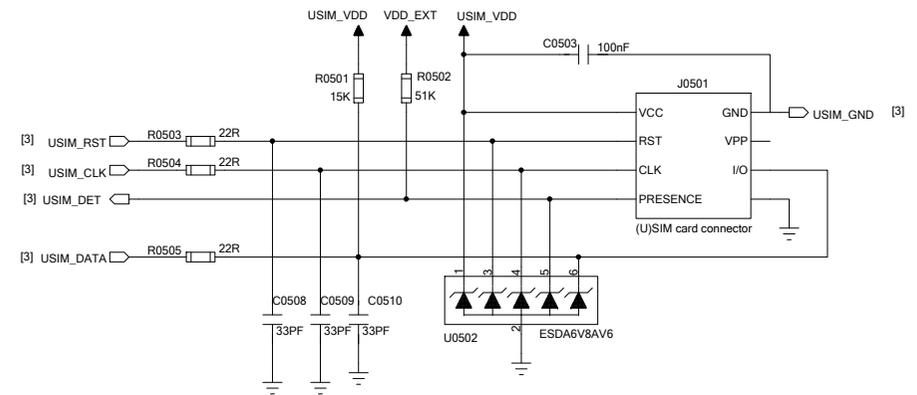
UART Level Translation - Transistor Solution



Notes:

- The IC solution is recommended as the top choice.
The transistor circuit solution is not suitable for applications with high baud rate exceeding 460 kbps.
- The voltage range of VCCA should not exceed that of VCCB. For more information about TXS0108E, please refer to the datasheet obtained from TI.
- For applications with high baud rate, it is highly recommended to install 1 nF capacitors (C0504 to C0507) on transistor circuits.
- The MAIN_DTR transistor circuit is similar to that of MAIN_RTS interface. The MAIN_RI and MAIN_DCD transistor circuits are similar to those of MAIN_CTS interface.

(U)SIM Interface



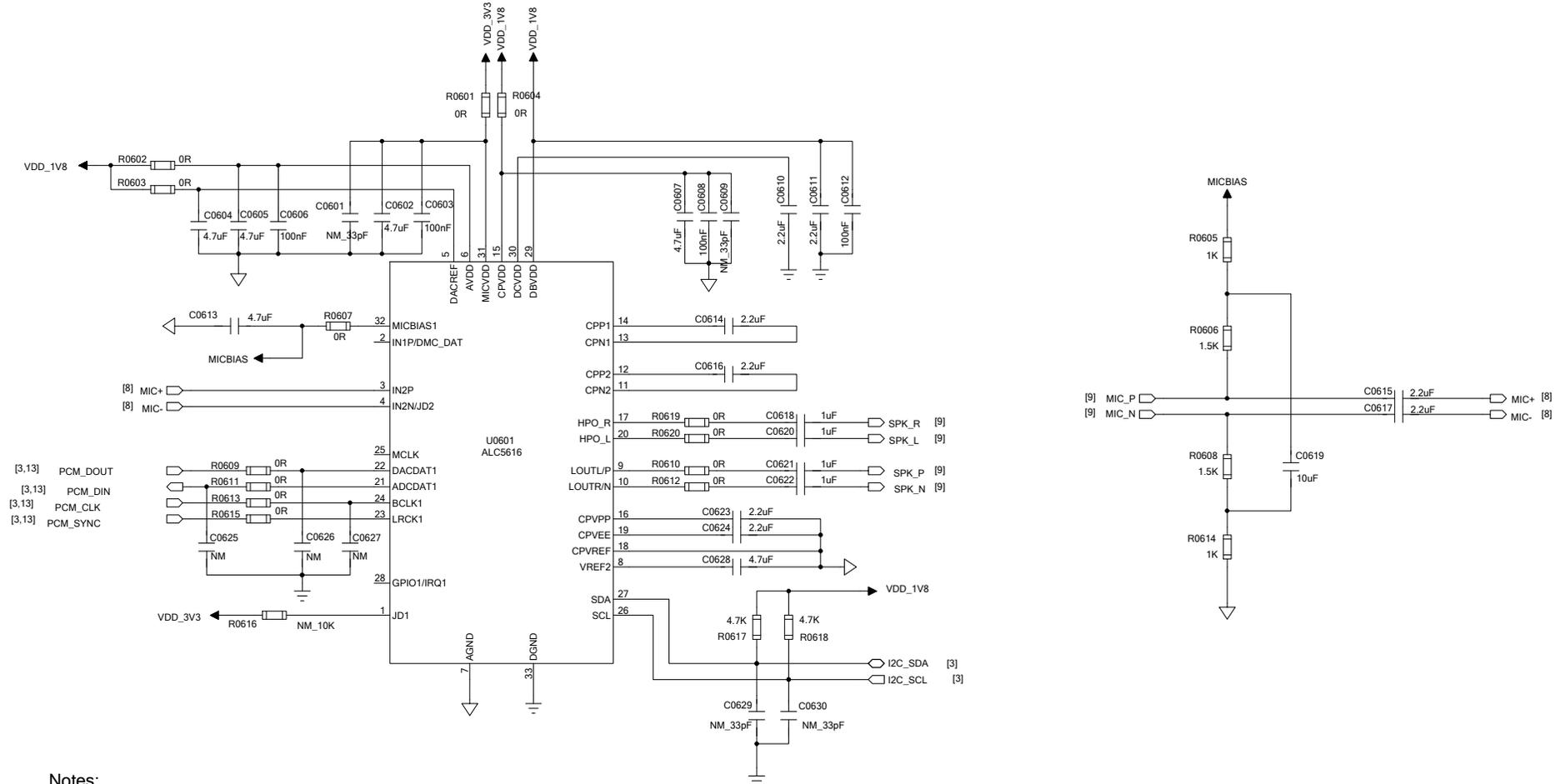
Notes:

- The decoupling capacitor of USIM_VDD should be less than 1 μ F and must be close to (U)SIM card connector.
- The module provides an input pin (USIM_DET) to detect (U)SIM card. It supports both low level and high level detection. Please refer to *Quectel_EG060V-EA_Hardware_Design* for more details.
- R0503 to R0505 are applied to suppress EMI spurious transmission and enhance ESD protection.
- It is recommended to take ESD protection measures near the (U)SIM card.
The TVS diode with a junction capacitance of less than 15 pF must be placed as close to the (U)SIM card connector as possible.
- R0501 improves anti-jamming capability of the (U)SIM circuit and it should be placed close to the (U)SIM card connector.
- The bypass capacitors C0508 to C0510 are reserved and not mounted by default.

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Audio Codec Design (ALC5616)



[3,13] PCM_DOUT
 [3,13] PCM_DIN
 [3,13] PCM_CLK
 [3,13] PCM_SYNC

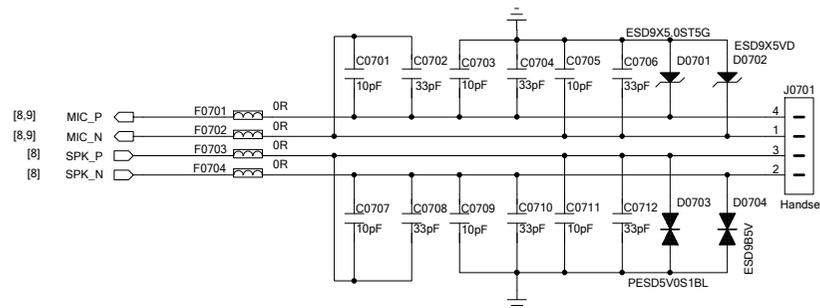
Notes:

1. ALC5616 power-on sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD -> MICVDD -> software initialization.
2. ALC5616 power-off sequence: disable codec function by software -> MICVDD -> DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. The module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be powered on before that.
4. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805, which is shown in the next page "Audio Interface Design".

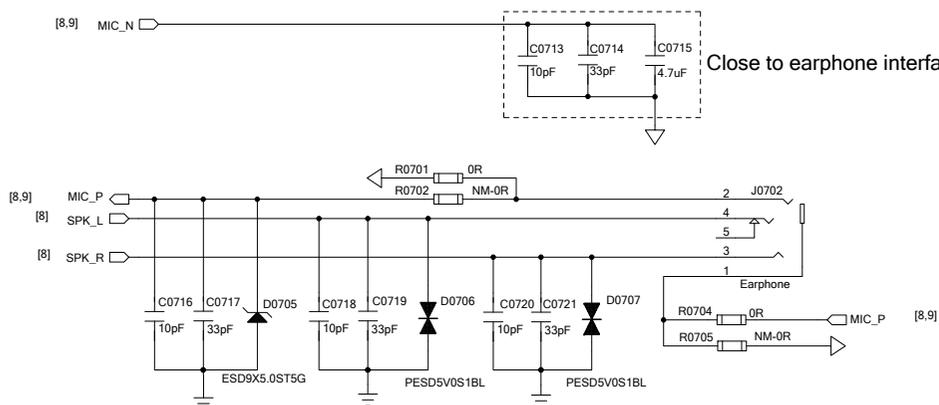
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Audio Interface Design

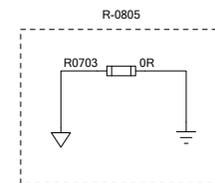
Handset Application



Earphone Application



	CTIA	OMTP
R0702/R0705	NM	M
R0701/R0704	M	NM



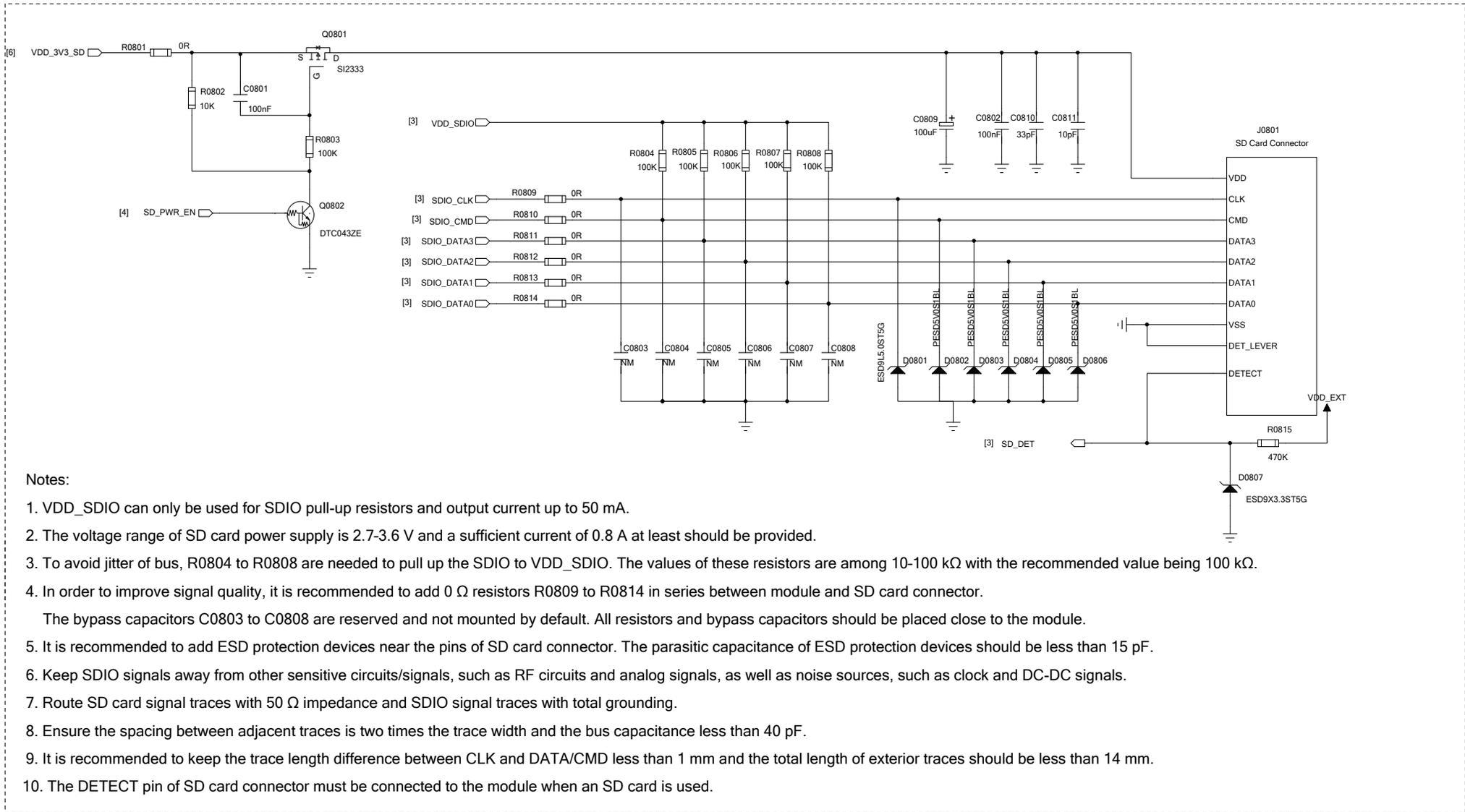
Notes:

1. The analog output only drives earphone and headset. For loads with higher power consumption such as speakers, an audio power amplifier should be added.
2. For handset application, route the MIC and SPK signal traces as differential pairs respectively.
3. For earphone application, route the MIC signal traces as a differential pair.
4. All MIC and SPK signal traces should be routed with total grounding and kept away from noise sources such as clock and DC-DC signals.

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SD Card Interface Design



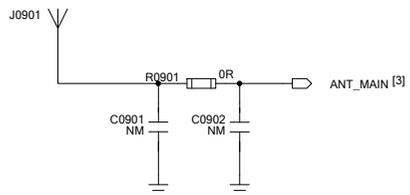
Notes:

- VDD_SDIO can only be used for SDIO pull-up resistors and output current up to 50 mA.
- The voltage range of SD card power supply is 2.7-3.6 V and a sufficient current of 0.8 A at least should be provided.
- To avoid jitter of bus, R0804 to R0808 are needed to pull up the SDIO to VDD_SDIO. The values of these resistors are among 10-100 kΩ with the recommended value being 100 kΩ.
- In order to improve signal quality, it is recommended to add 0 Ω resistors R0809 to R0814 in series between module and SD card connector.
The bypass capacitors C0803 to C0808 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- It is recommended to add ESD protection devices near the pins of SD card connector. The parasitic capacitance of ESD protection devices should be less than 15 pF.
- Keep SDIO signals away from other sensitive circuits/signals, such as RF circuits and analog signals, as well as noise sources, such as clock and DC-DC signals.
- Route SD card signal traces with 50 Ω impedance and SDIO signal traces with total grounding.
- Ensure the spacing between adjacent traces is two times the trace width and the bus capacitance less than 40 pF.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1 mm and the total length of exterior traces should be less than 14 mm.
- The DETECT pin of SD card connector must be connected to the module when an SD card is used.

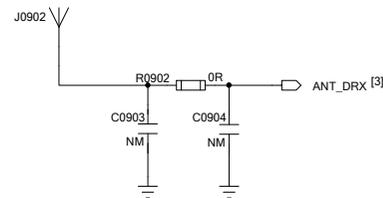
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RF Antenna Design

Main Antenna Interface



Diversity Antenna Interface



Notes:

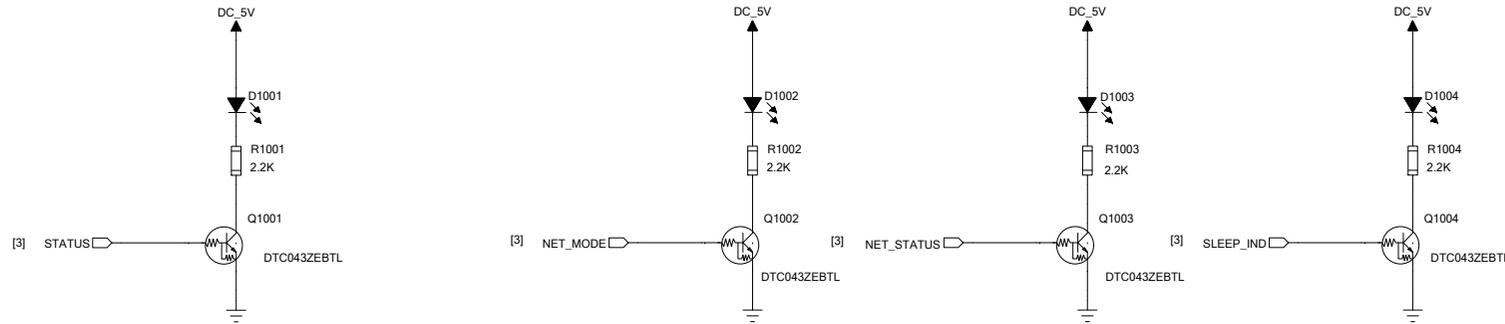
1. The n type circuit is recommended for main antenna and diversity receiving antenna to facilitate future debugging.
2. The diversity reception function is ON by default.
3. While routing, keep the impedance of RF signal traces at 50 Ω.

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Other Designs

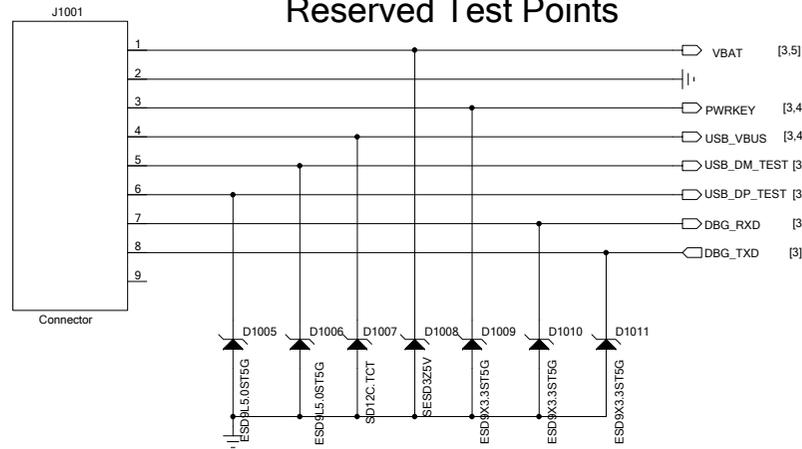
Indicators



Notes:

- For more details about NET_MODE and NET_STATUS, please refer to *Quectel_EG060V-EA_Hardware_Design*.
- If the current consumption is required to be as low as possible when the device is in sleep mode, replace the power supply of indicators with a controllable one, which can be turned off when the module enters sleep mode.

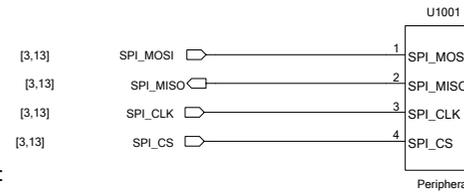
Reserved Test Points



Notes:

- Both USB and debug UART interfaces are reserved for software debugging.
 - USB interface can also be used to upgrade firmware.
 - Keep USB test points as close to USB pins as possible.
 - Please note that the junction capacitance of ESD protection components on USB data traces might affect the signal quality. Typically, the capacitance should be kept less than 1 pF.
 - Debug UART interface supports 1.8 V power domain.
- A level translator should be used if the power domain of your application is 3.3 V.

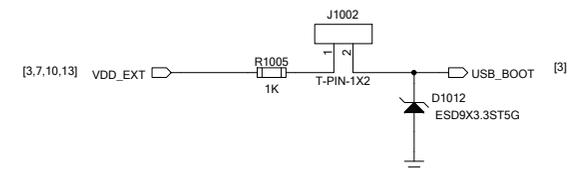
SPI Connection



Note:

SPI only supports the master mode.

Emergency Download Mode



Note:

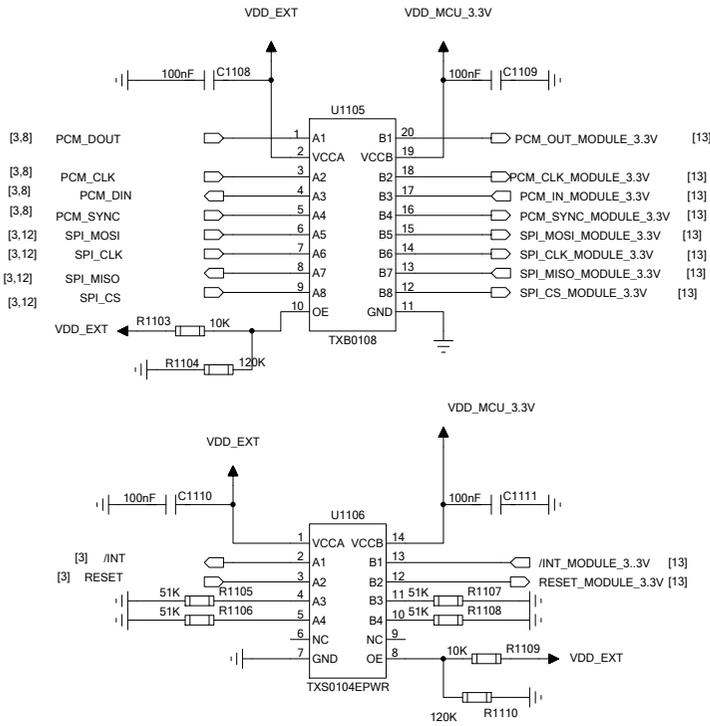
USB_BOOT is enabled by default and the module will be forced into download mode when USB_BOOT is at high level.

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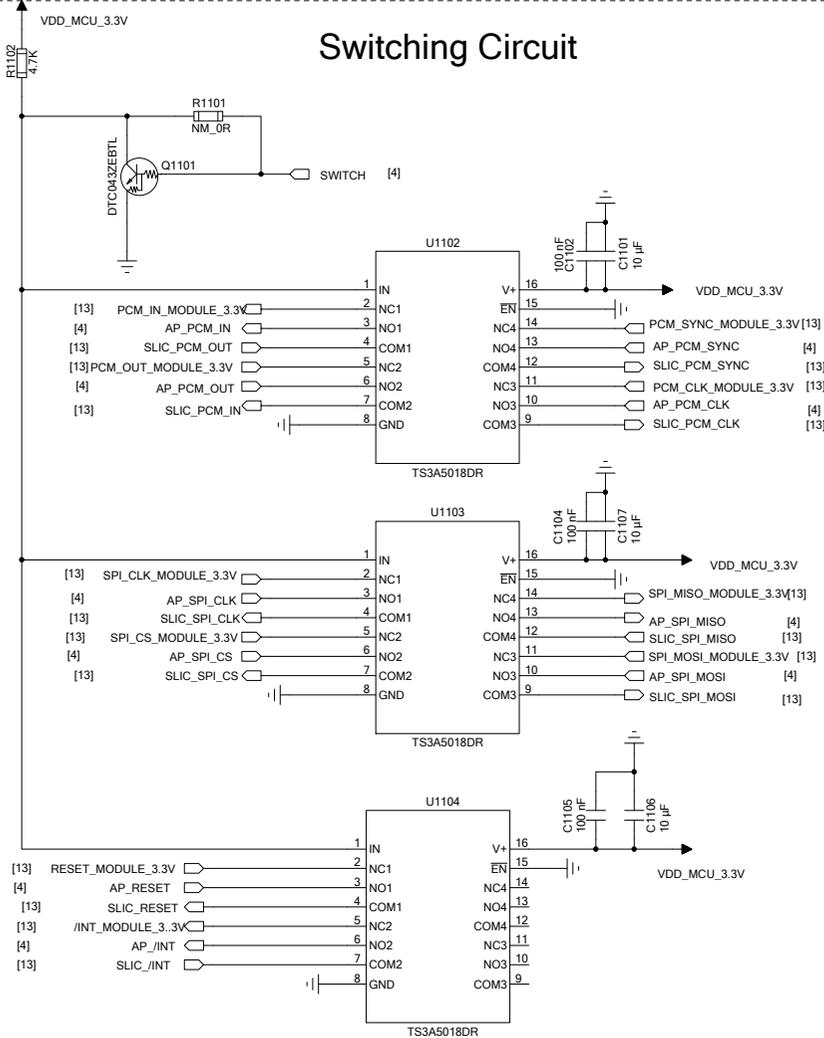
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SLIC Design

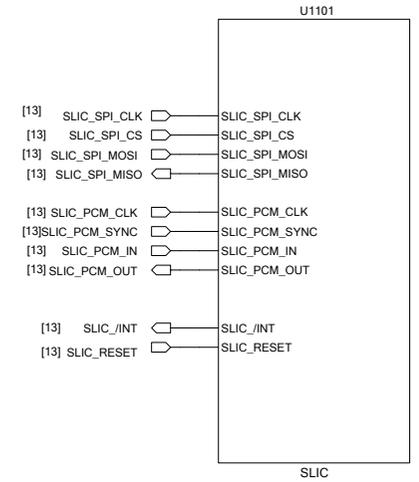
Level Matching Circuit



Switching Circuit



SLIC Interface



Notes:

1. The I/O level of the module is 1.8 V.
2. Please pay attention to I/O level matching.

\overline{EN}	IN	COM TO NO	COM TO NC	Where is the SLIC chip connected
Low	Low	OFF	ON	EG060V-EA
Low	High	ON	OFF	AP
High	X	OFF	OFF	X

Notes:

1. When the SLIC chip is connected to the module, the module picks up VoLTE function
2. When the SLIC chip is connected to AP chip, the AP picks up VoIP function.

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