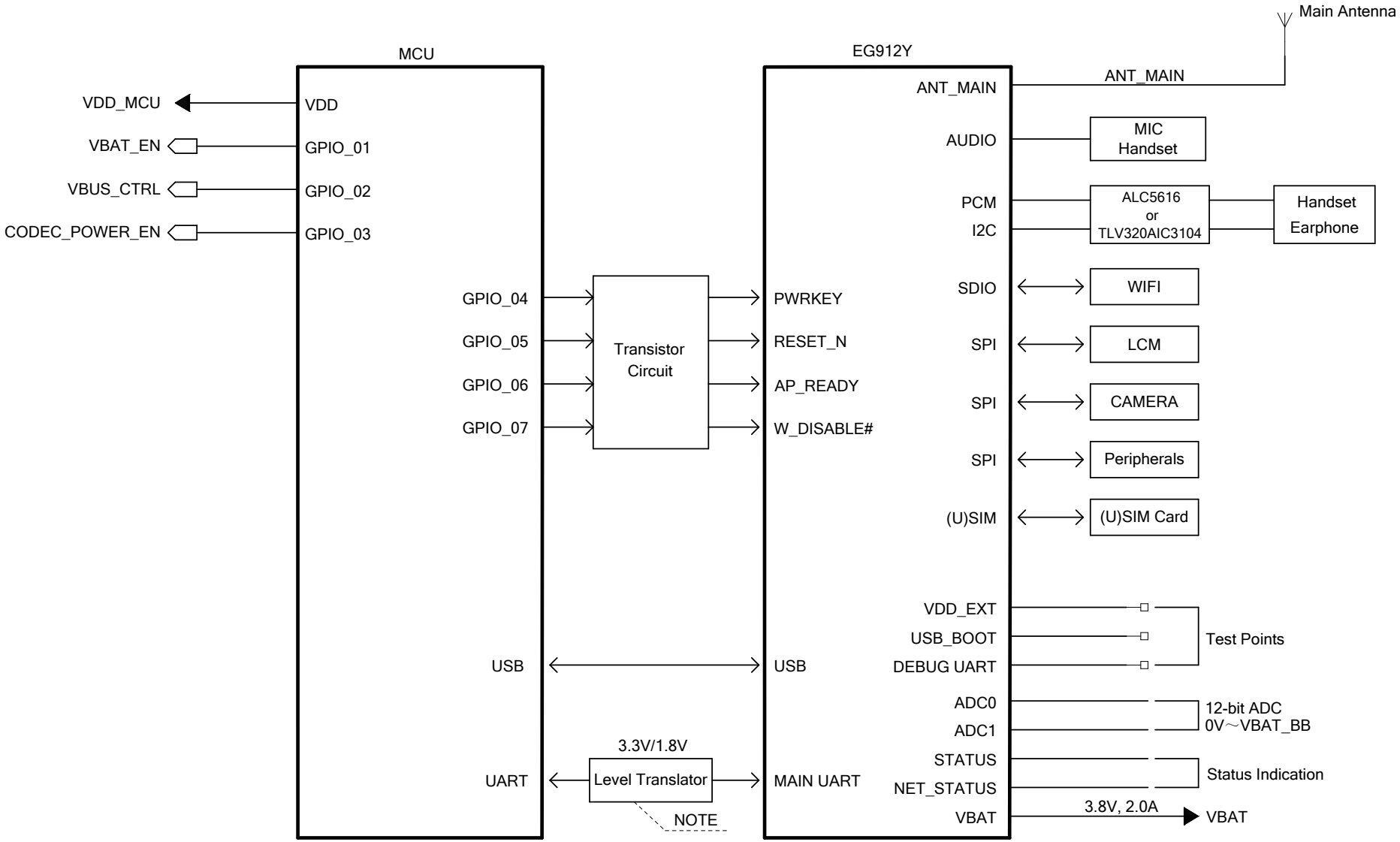
Block Diagram



NOTE:
A transistor translation circuit or a level translator TXS0108EPWR provided by Texas Instruments is recommended.

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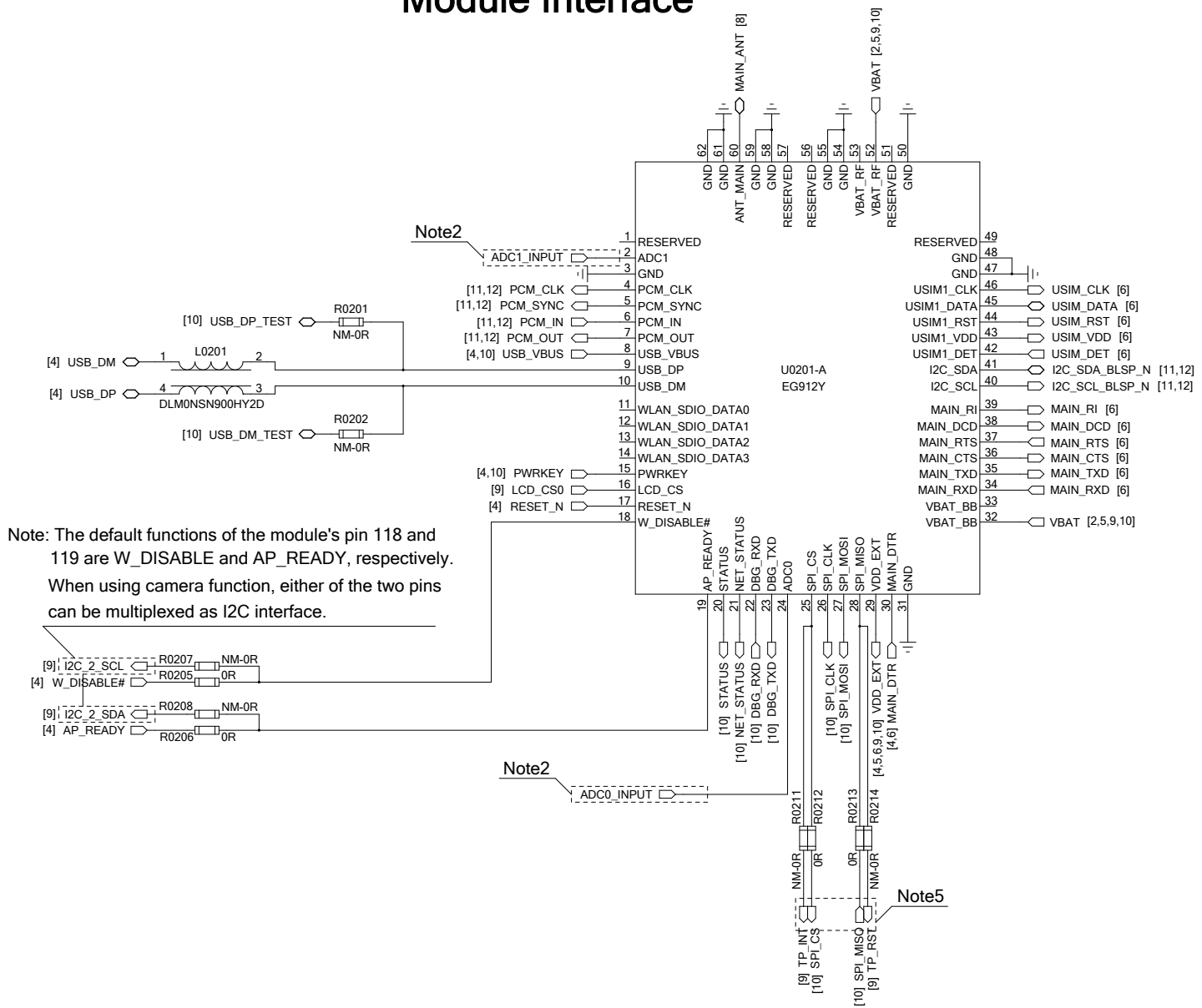
Module Interface



Note :

1. It is recommended to reserve USB upgrade test points and keep the branch traces as short as possible, and the resistors R0201 ~ R0202 should be close to the module's USB interface.
2. ADC0&ADC1 input range is 0 ~ VBAT_BB.If the acquisition voltage exceeds VBAT_BB. It is recommended to use voltage divider resistor input.
3. The STATUS and USB_BOOT pins must not be pulled up until the module is successfully powered on.
4. The default functions of the module's pin 125 and 128 are SPI interface, It can also be configured as a normal GPIO interface.

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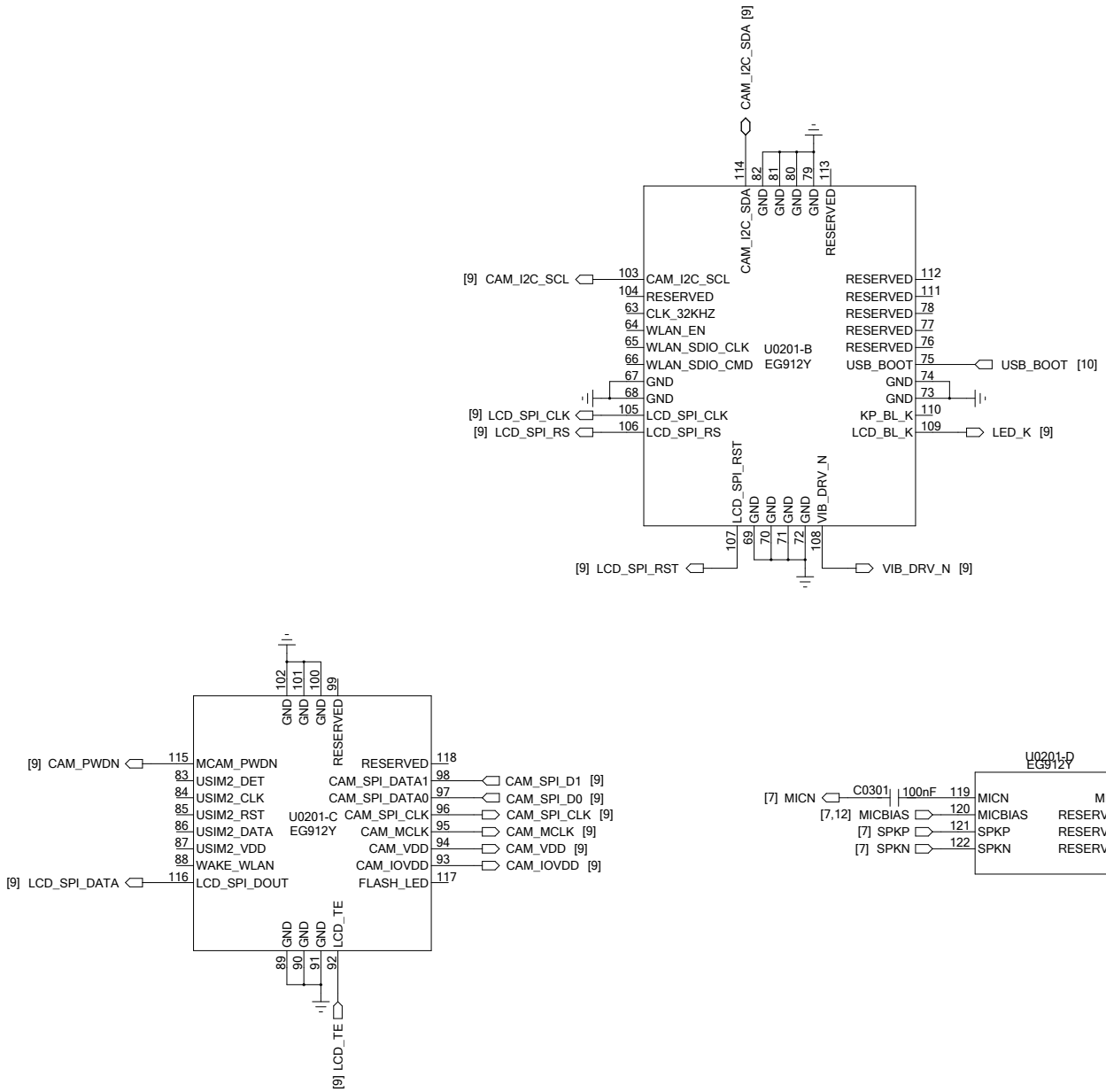

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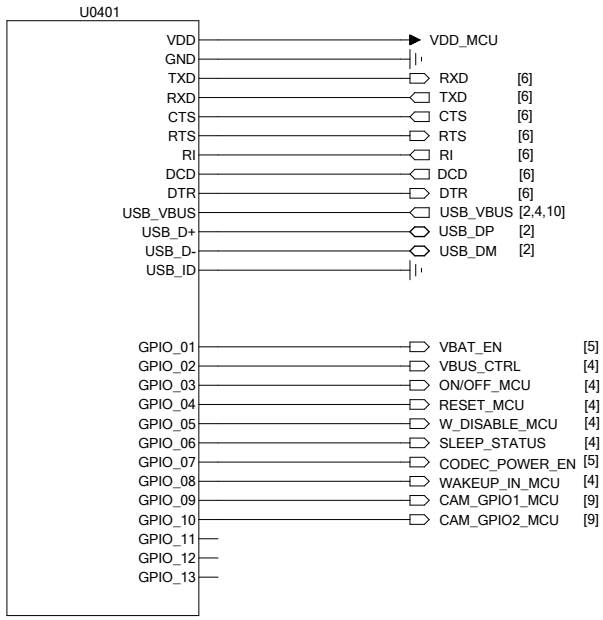
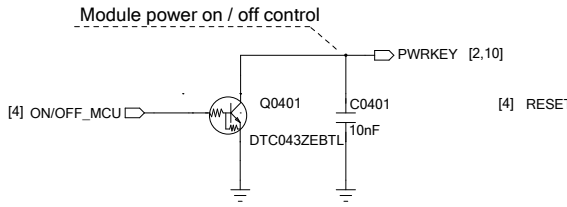
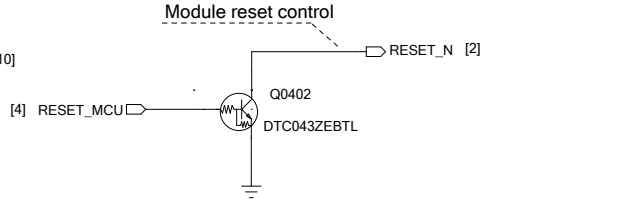
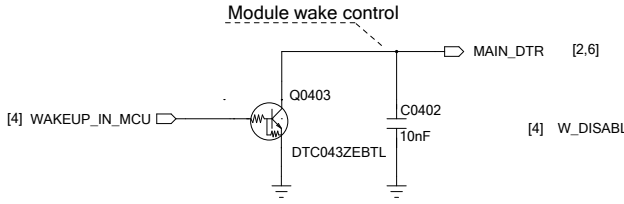
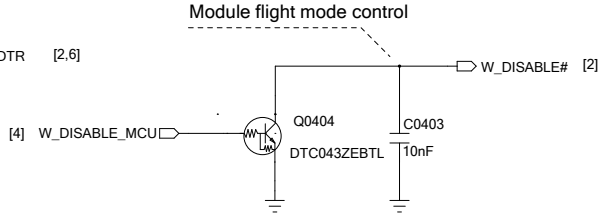
Driver Circuit

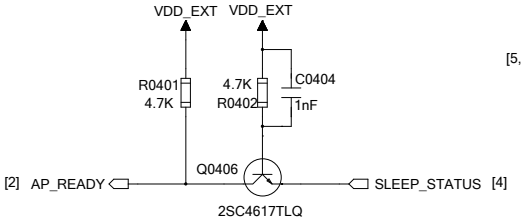


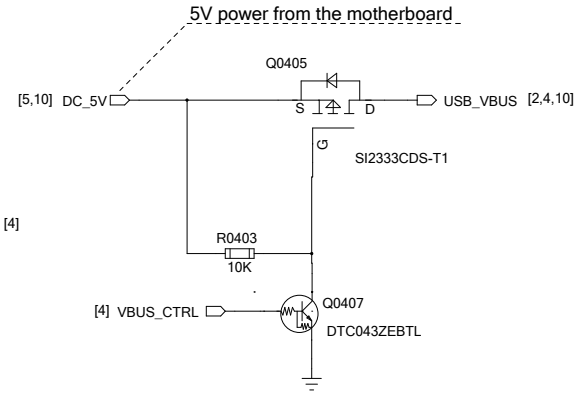












Note :

1. U0401 refers to the customer's controller. The module's GPIO type interface is a 1.8V voltage domain. If the U0401's GPIO is 1.8V, the related level shifting circuit is not needed.
2. The module's USB can only be used as a slave device and supports USB2.0 high-speed and full-speed modes. Therefore, the host controller must support the USB host or OTG function.
   The module and the host controller's USB_VBUS are used as input sources and need to be provided externally.
   The VBUS of the module is a USB detection function and a USB charging function, and the maximum charging current is 1A.
   VBUS_CTRL is used to control the power on and off of USB_VBUS.
3. AP_READY is used to detect the sleep state of the main controller.

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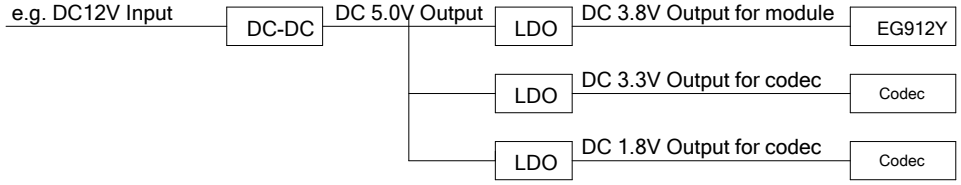
Power Design

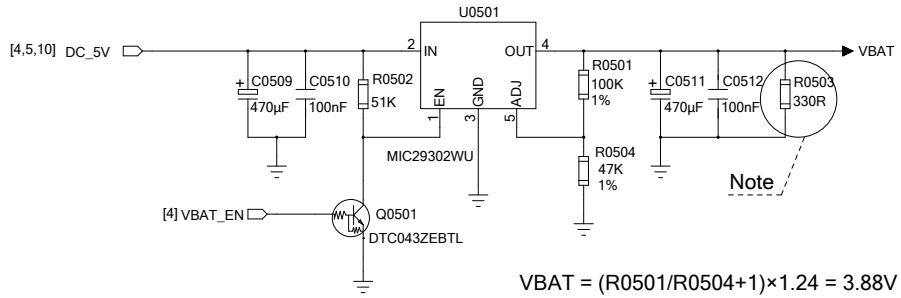
DC-DC Application

When the input voltage exceeds 7V, use DC-DC to convert the input voltage to 5V and generate 3.8V through the LDO.



LDO Application

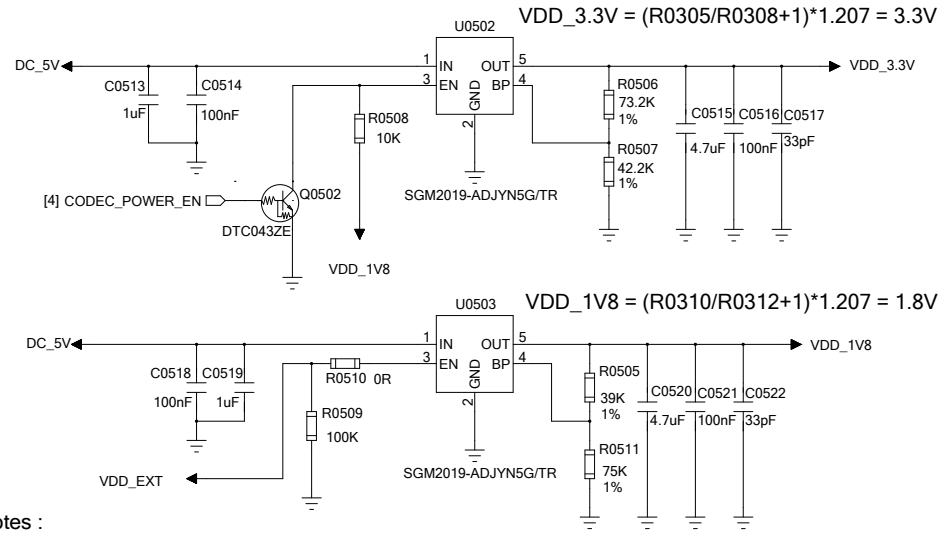
When the input voltage is lower than 7.0V, the LDO can generate 3.8V to power the module.



VBAT = (R0501/R0504+1)×1.24 = 3.88V

Note: The recommended load current is not less than 10mA.

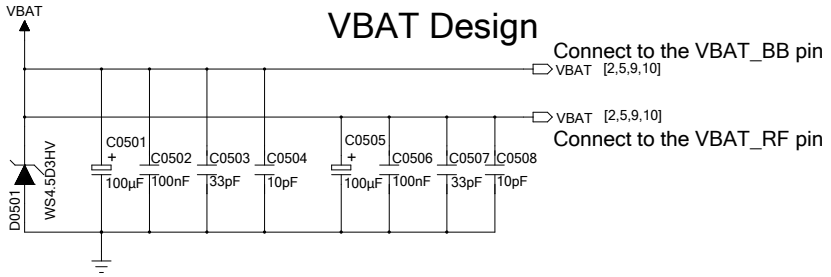
Supply Power for PCM Codec



Notes :

1. CODEC_POWER_EN must be at low level in order to ensure the normal output voltage of VDD_3.3V. If VDD_3.3V power supply needs to be switched off, please keep CODEC_POWER_EN at high level.
2. The following power-on/off sequences should be complied with to ensure the audio codec works normally.
   Power-on Sequence: power on VDD_1V8 first, then VDD_3.3V.
   Power-off Sequence: power off VDD_3.3V first, then VDD_1V8.

VBAT Design



Notes :

1. VBAT supply current must meet the rated output capacity of 2.0A.
2. The VBAT trace should be connected to pins VBAT_BB and VBAT_RF in a star structure.
3. Typical VBAT operating voltage is 3.8V.
4. Capacitance is arranged in ascending order, the smallest one closes to the VBAT pad, and keep all capacitance as close to the VBAT pad as possible.

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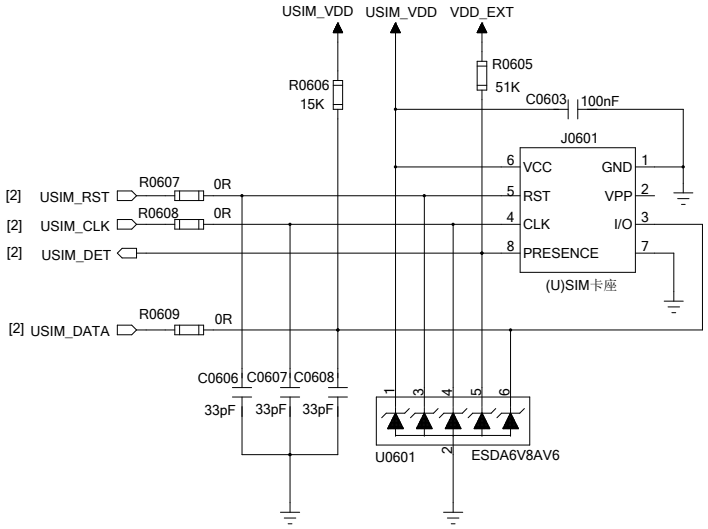
(U)SIM&UART Interfaces

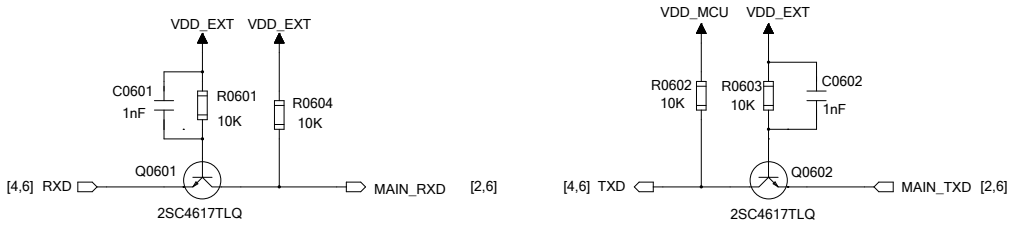
(U)SIM Interface



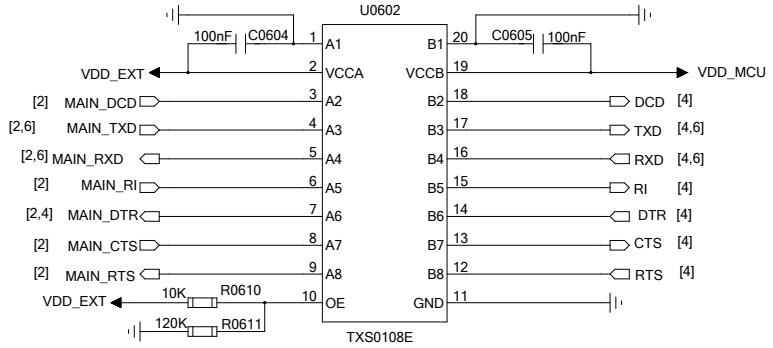
Notes:

1. U0601 is used for protecting (U)SIM card against ESD, and the junction capacitance should be less than 15pF.
2. The pull-up resistor R0606 helps to improve the anti-interference performance of the (U)SIM card.
   It is recommended to place it close to the (U)SIM card connector.
3. The capacitance of C0603 should be less than 1μF.

Serial Triode Conversion Scheme



Serial Conversion Chip Solution



Notes:

1. The level conversion circuit of the serial port in this design provides a triode conversion scheme and a serial port conversion chip scheme. It is recommended to use a serial port conversion chip scheme.
2. TXS0108E requires that VCCA must be less than or equal to VCCB.
   For more design details, please refer to the TXS0108E chip data sheet.
3. The triode solution is suitable for applications where the baud rate is lower than 460Kbps.
   The 1nF capacitor helps improve the signal quality.
4. RTS and DTR transistor level shifting circuits are the same as RXD circuits.
   The CTS, RI, and DCD transistor level-shifting circuits are the same as the TXD circuit.

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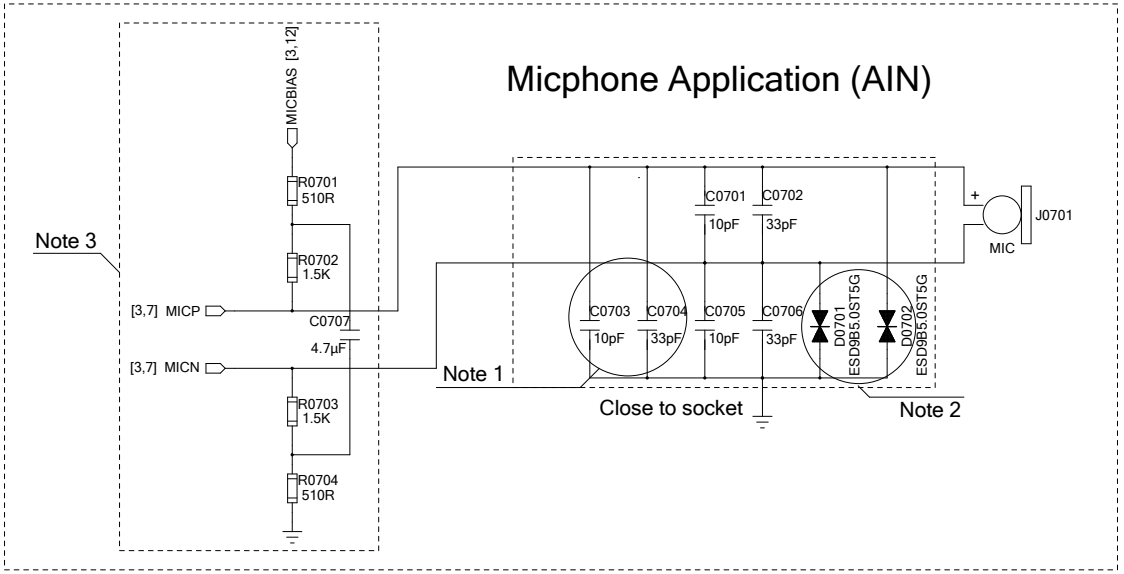
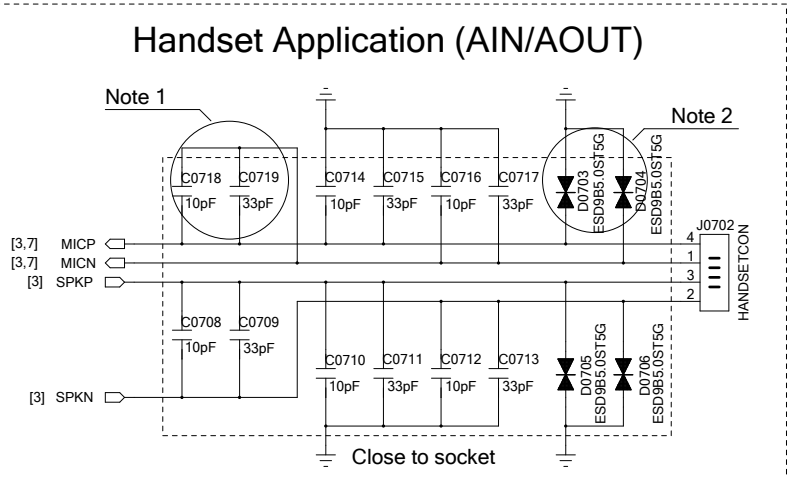
Analog Audio Interfaces

Micphone Application (AIN)



Handset Application (AIN/AOUT)



Notes:

1. 10pF and 33pF capacitors are used to filter TDD noise.
2. Components D0701, D0702, D0703, D0704, D0705, D0706 are used for ESD protection of MIC signal lines, and are thus strongly recommended to be reserved.
3. When using an electret microphone, an external bias circuit is required.

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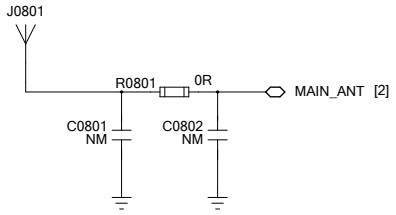
Antenna

Main Antenna



Note :

The impedance of main antenna is 50Ω.

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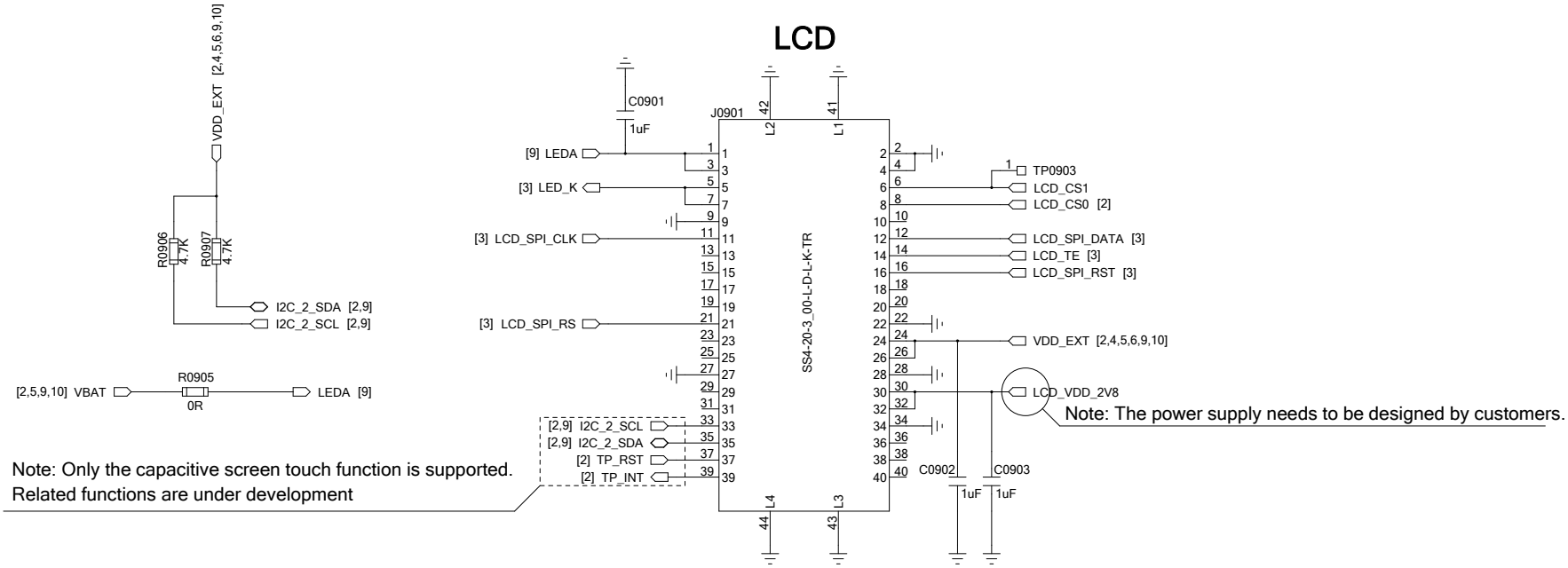
LCD&Camera&Motor

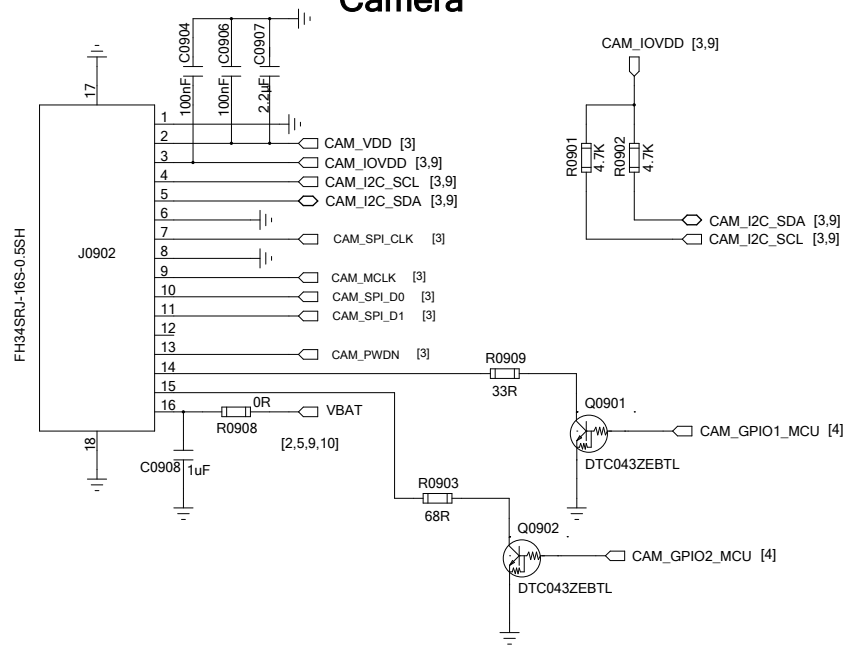
LCD



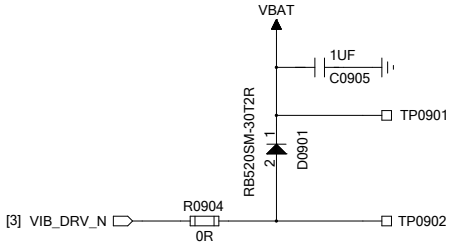
Note: Only the capacitive screen touch function is supported.
Related functions are under development

Note: The power supply needs to be designed by customers.

Camera



Motor



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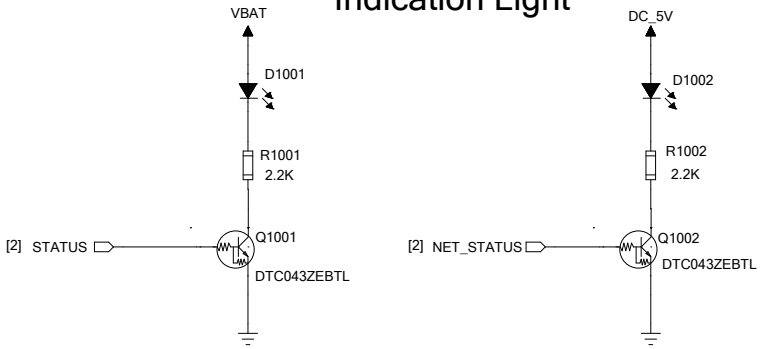
Other Designs

Indication Light

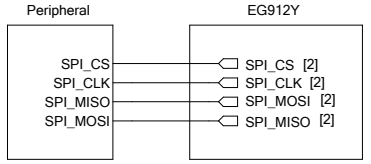


Note:

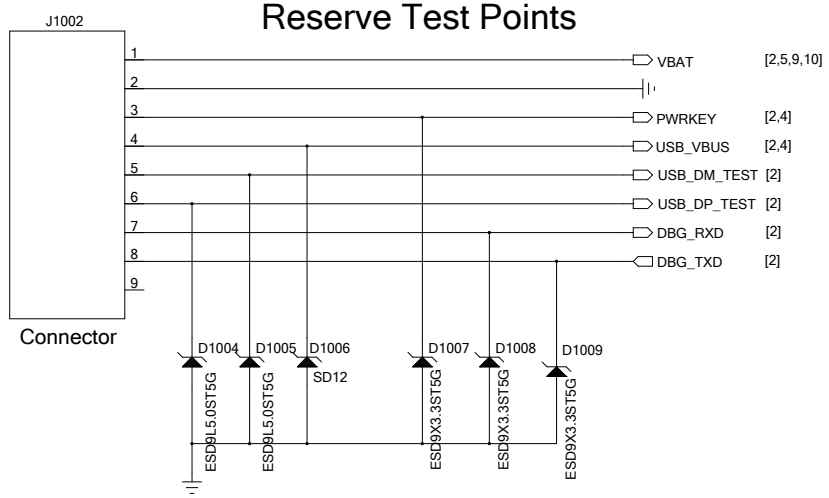
When the client has a requirement for the sleep current of the entire machine, the STATUS and NET_STATUS indicators can be powered on.

VBAT and DC_5V are replaced with external controllable power supply and shut down when the module sleeps to reduce the sleep power consumption.

SPI Connection



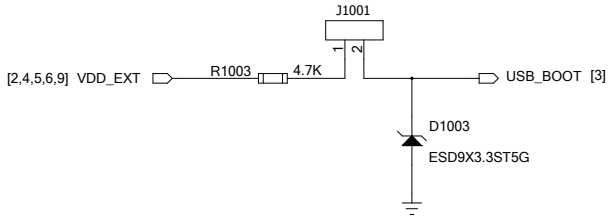
Reserve Test Points



Notes :

1. Test points for both USB and debug UART interfaces are reserved for capturing logs.
2. Test points of USB interface can also be reserved for module firmware upgrade.
3. The ESD parasitic capacitance on the USB signal line should be less than 2pF.
4. The Debug UART interface level is 1.8V, and a level conversion chip is required when connecting to a 3.3V system.

USB_BOOT Interface



Notes :

1. It is strongly recommended to reserve the USB_BOOT design.
2. USB_BOOT is kept open by default. When it is at high level, it forces the module to enter the download mode.

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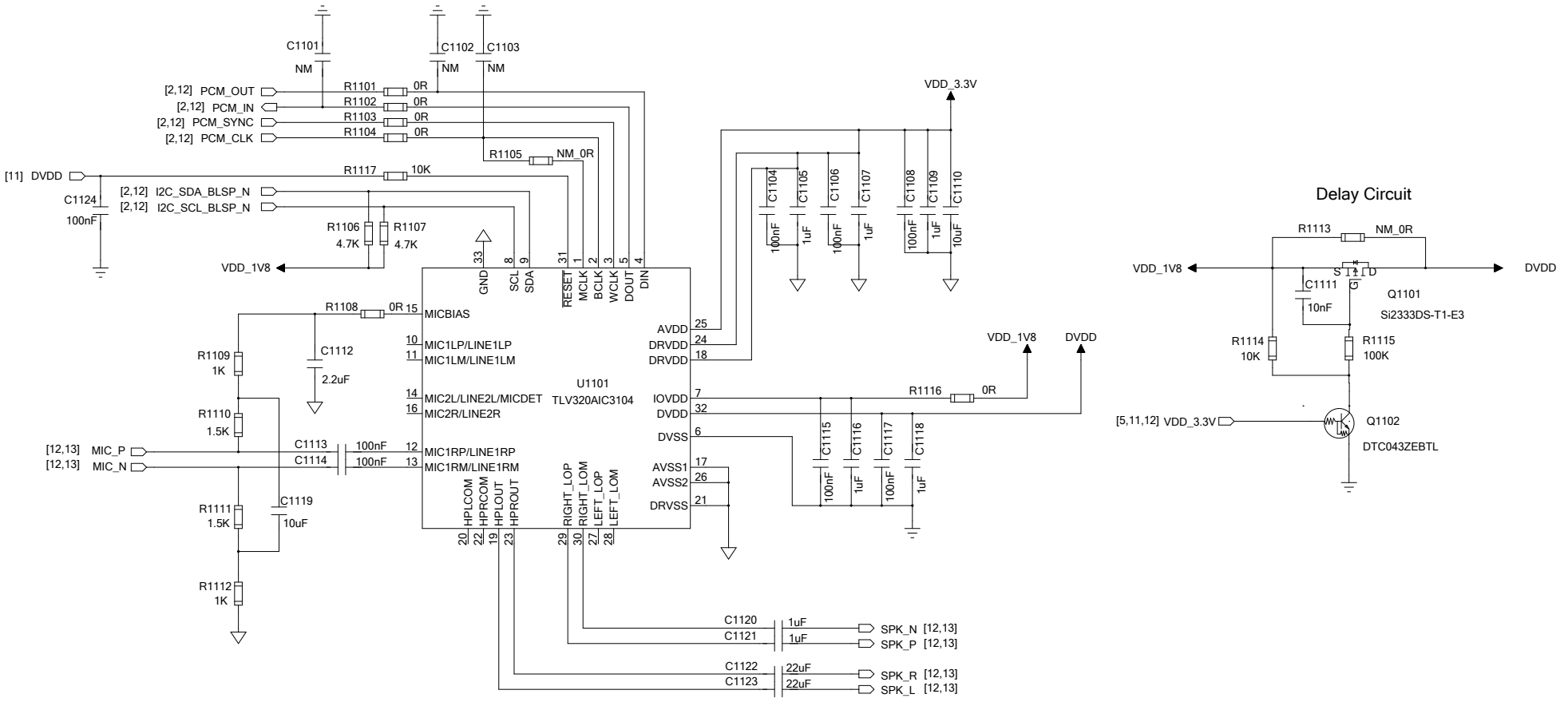
Audio Codec Design (TLV320AIC3104)



Notes:

1. TLV320AIC3104 power-on sequence: IOVDD -> AVDD/DRVDD -> DVDD -> software initialization.
2. The RC delay circuit, which is assembled with C0612 and R0612, is used to enure that the power on time difference between AVDD and DVDD is within 5ms.
3. The RESET pin must be driven at low level for at least 10ns after all power supplies for TLV320AIC3104 are at their specified values.
4. Attention needs to be paid to the distinction between analog and digital land.
5. Please refer to the TLV320AIC3104 device specification for more details.

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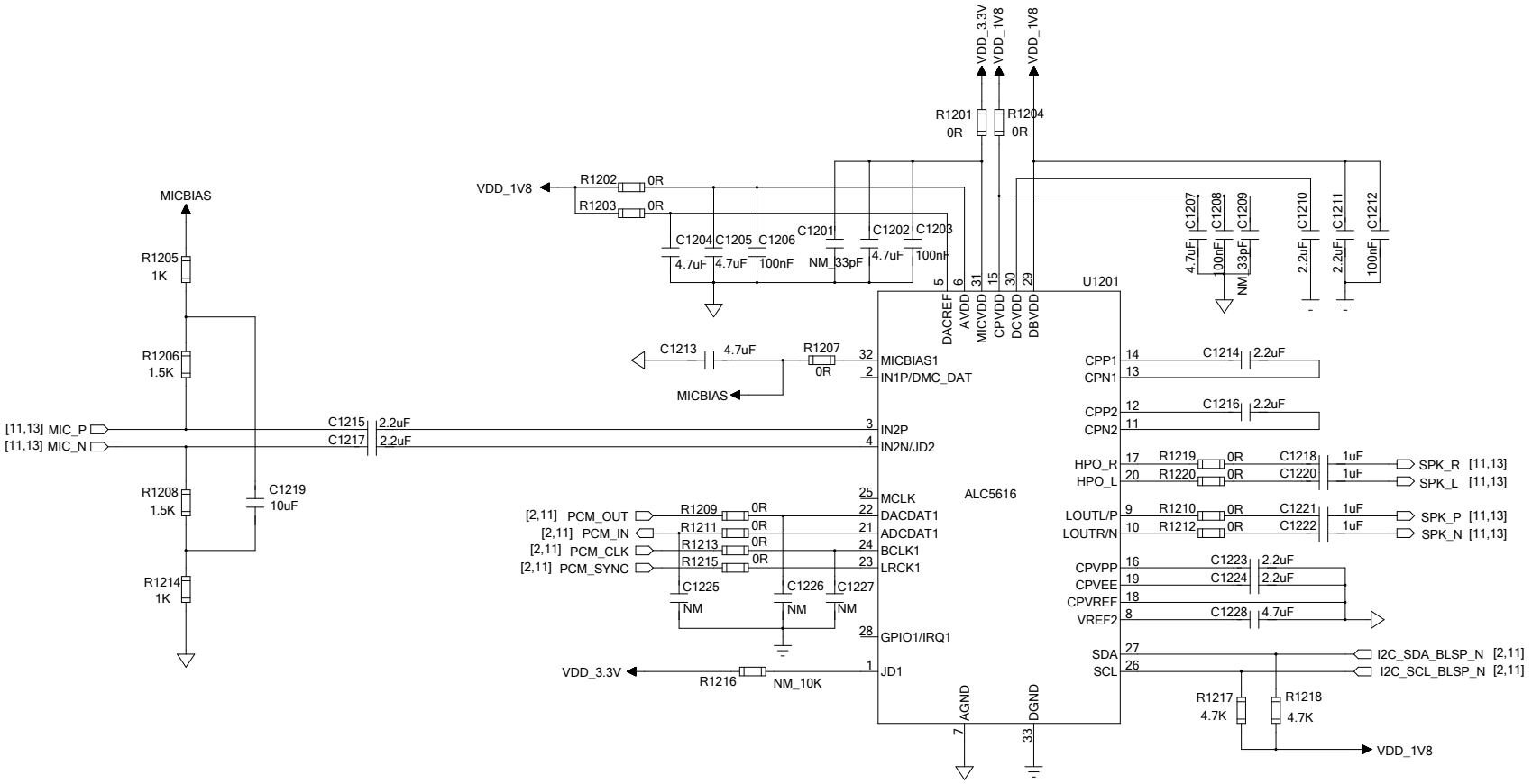
Audio Codec Design (ALC5616)



Notes:

1. ALC5616 power-on sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD -> MICVDD -> software initialization.

2. ALC5616 power-off sequence: close codec function by software -> MICVDD -> DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.

3.Attention needs to be paid to the distinction between analog and digital land.

4.Please refer to the ALC5616 device specification for more details.

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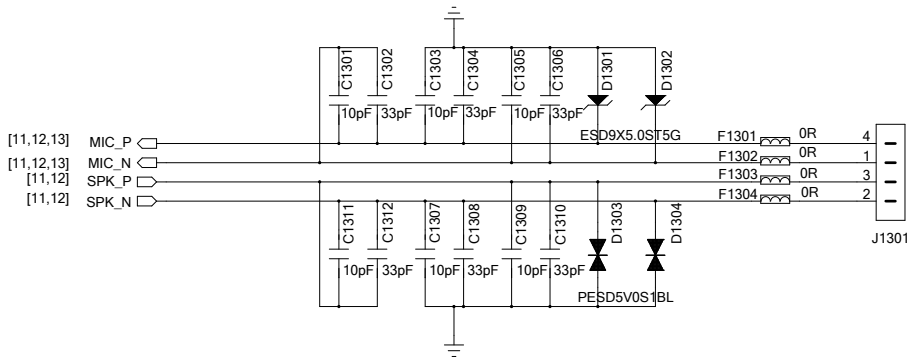
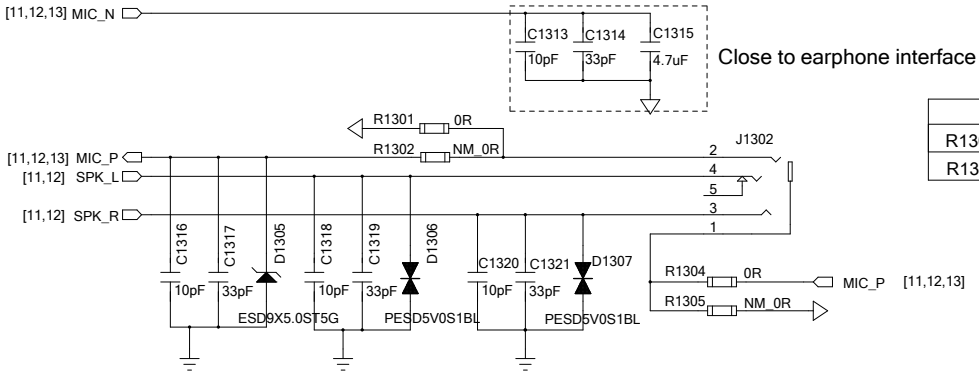
Codec Audio Interfaces

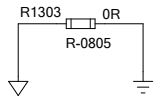
Handset Application (AIN/AOUT)



Earphone Application (AIN/AOUT)



	CTIA	OMTP
R1302/R1304	NM	M
R1301/R1303	M	NM



Notes:

1. The analog output only drives earphone and headset. For larger power loads such as speakers, an audio power amplifier should be added in the design.
2. In handset application, route the MIC and SPK signal traces as differential pairs respectively.
3. In earphone application, route the MIC signal traces as differential pairs.
4. All MIC and SPK signal traces should be routed with total grounding and far away from noise such as clock and DC-DC signals, etc.
5. ALC5616 and TLV320AIC3104 cannot be used simultaneously in audio codec.

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