EG9x&BG96&UG96&UG95 Compatible Design

UMTS/HSPA/LTE Module Series

Rev. EG9x&BG96&UG96&UG95_Compatible_Design_V1.0

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www.quectel.com

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Quectel Wireless Solutions Co., Ltd.
Office 501, Building 13, No.99, Tianzhou Road, Shanghai, China, 200233
Tel: +86 21 5108 6236
Email: info@quectel.com

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About the Document

History

Revision	Date	Author	Description
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1 Introduction

Quectel EG9x module is pin-to-pin compatible with Quectel LTE Cat.M1/NB1 BG96 module and UMTS/HSPA UG96 and UG95 modules. This document briefly describes the compatible design among EG9x, BG96, UG96 and UG95 modules.

In this document, EG9x refers to Quectel EG95 and EG91 modules.

2 General Descriptions

2.1. Product Description

UG96 and UG95 are UMTS/HSPA modules, and UG95 includes two variants: UG95-A and UG95-E. BG96 module is a series of embedded IoT (LTE Cat.M1/Cat.NB1/EGPRS) wireless communication module without receive diversity and it supports Half-Duplex LTE-FDD/TDD wireless communication. EG9x is a series of embedded 4G wireless communication module with receive diversity. It supports LTE-FDD/WCDMA/GSM wireless communication, and provides data connectivity on LTE-FDD, DC-HSPA+, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. EG9x, BG96, UG96 and UG95 are designed as pin-to-pin compatible products. Customers can choose a proper module according to specific application demands. The compatible design guideline ensures a smooth migration from UG96/UG95 to BG96/EG9x for customers' products.

Table 1: Module General Information

Module	Appearance	Packaging	Dimensions (mm)	Description
EG9x		102-pin LGA	29 × 25 × 2.3	LTE-FDD/WCDMA/GSM module
BG96		102-pin LGA	26.5 × 22.5 × 2.3	LTE Cat.M1/Cat.NB1/EGPRS module

UG96		102-pin LGA	26.5 × 22.5 × 2.2	UMTS/HSPA module
UG95		102-pin LGA	23.6 × 19.9 × 2.2	UMTS/HSPA module

2.2. Features Overview

The following table compares general properties and features of EG9x, BG96, UG96 and UG95 modules.

Table 2: Features Overview

Feature	UG95	UG96	BG96	EG9x
Power Supply	3.3V~4.3V Typ. 3.8V	3.3V~4.3V Typ. 3.8V	3.3V~4.3V Typ. 3.8V	3.3V~4.3V Typ. 3.8V
Peak Current	VBAT_BB: Max 0.8A VBAT_RF: Max 2.0A	VBAT_BB: Max 0.8A VBAT_RF: Max 2.0A	TBD	VBAT_BB: Max 0.8A VBAT_RF: Max 2.0A
Sleep Current	**2G:** 1.12mA @DRX=5 **3G:** 1.98mA @DRX=6	**2G:** 1.1Ma @DRX=5 **3G:** 2.52mA @DRX=6	TBD	TBD
Frequency Bands	**UG95-A:** UMTS: 850/1900MHz **UG95-E:** GSM: 900/1800MHz UMTS: 900/2100MHz	GSM: 850/900/ 1800/1900MHz UMTS: 800/850/900/ 1900/2100MHz	Cat.M1 & NB1: LTE-FDD: B1/B2/B3/B4/ B5/B8/B12/ B13/B18/B19/ B20/B26/B28 LTE-TDD: B39 *(B39 for Cat.M1 only)* GSM850/GSM900/	GSM:900/1800MHz WCDMA: B1/B8 LTE-FDD: B1/B3/B7/B8/B20/ B28A*

			DCS1800/PCS1900	
UMTS/HSPA	Supported	Supported	Not supported	Supported
LTE-FDD	Not supported	Not supported	Supported	Supported
EDGE	Multi-slot class 12 Downlink only	Multi-slot class 33	Multi-slot class 33	Multi-slot class 33
GPRS	Multi-slot class 12	multi-slot class 33	Multi-slot class 33	Multi-slot class 33
Temperature Range	Operation temp. range: -35 ~ +75°C [1)] Extended temp. range: -40 ~ +85°C [2)]	Operation temp. range: -35 ~ +75°C [1)] Extended temp. range: -40 ~ +85°C [2)]	Operation temp. range: -35 ~ +75°C [1)] Extended temp. range: -40 ~ +85°C [2)]	Operation temp. range: -35 ~ +75°C [1)] Extended temp. range: -40 ~ +85°C [2)]
Serial Interface	Baudrate: 300 to 921600bps Autobauding: 4800 to 115200bps Flow control: RTS/CTS Signal level: 1.8V	Baudrate: 300 to 921600bps Autobauding: 4800 to 115200bps Flow control: RTS/CTS Signal level: 1.8V	Baudrate: 300 to 921600bps Autobauding: 4800 to 115200bps Flow control: RTS/CTS Signal level: 1.8V	Baudrate: 300 to 921600bps Autobauding: 4800 to 115200bps Flow control: RTS/CTS Signal level: 1.8V
USB Interface	USB 2.0, high speed	USB 2.0, high speed	USB 2.0, high speed	USB 2.0, high speed
SWD Interface	Not supported	Not supported	Not supported	Not supported
Analog Audio	Not supported	Not supported	Not supported	Not supported
Digital Audio	PCM	PCM	I2S*	PCM
ADC	Not supported	Not supported	Supported	Supported
RTC Backup	Vnorm=1.8V VI=1.0V~1.9V	Vnorm=1.8V VI=1.0V~1.9V	Not supported	Not supported
I2C Interface	Supported	Supported	Supported	Supported
SPI Interface	Not supported	Not supported	Not supported	Supported
(U)SIM Card Detection	Supported	Supported	Supported	Supported
Firmware Upgrade	USB, UART	USB, UART	USB, DFOTA*	USB, DFOTA*

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Pin Assignment

The following figure shows the pin assignment of EG9x, BG96, UG96 and UG95.

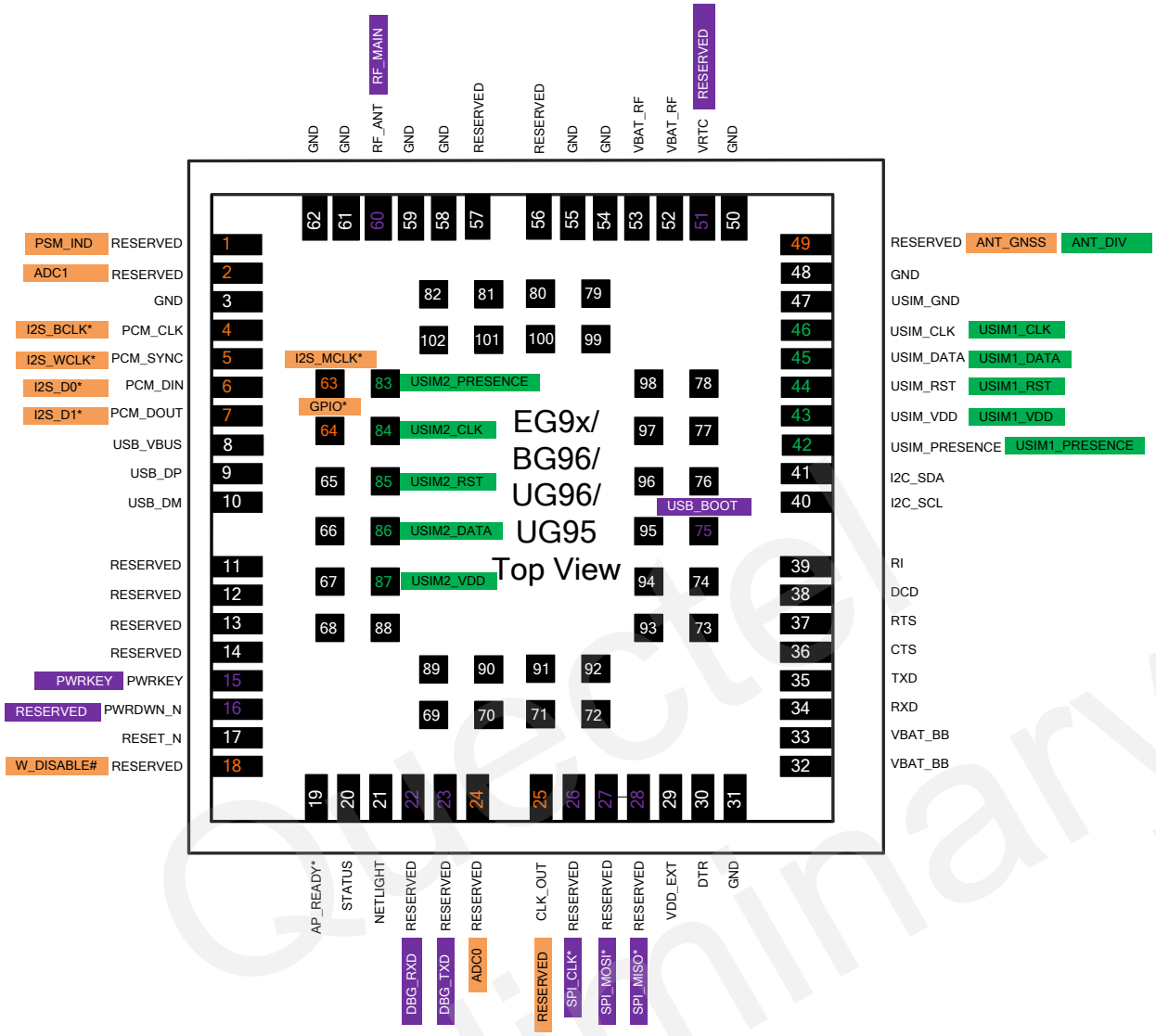

Figure 1: EG9x&BG96&UG96&UG95 Pin Assignment

NOTES

1. Green, purple and black colored pin names are for EG9x.
2. Orange, purple and black colored pin names are for BG96.
3. Black colored pin names are for UG96/UG95.
4. The green and orange colored pin names stand for different functional pins between EG9x and BG96.
5. The green and purple colored pin names stand for different functional pins between EG9x and EG96/UG95.
6. Pins 83~87 of EG9x are (U)SIM2 card interface.
7. For more details about the pins with different functions, please refer to ***Table 4***.

3 Pin Description

This chapter describes the pin definition of EG9x, BG96, UG96 and UG95, as well as the pin comparison among them.

Table 3: I/O Parameters Definition

Symbol	Description
IO	Bidirectional
DI	Digital Input
DO	Digital Output
PI	Power Input
PO	Power Output
AI	Analog Input
AO	Analog Output
OD	Open Drain

The following table shows the comparison of pins among EG9x, BG96, UG96 and UG95.

Table 4: Pin Comparison among EG9x, BG96, UG96 and UG95

Pin No.	UG96/UG95			BG96			EG9x		
	Pin Name	I/O	Description	Pin Name	I/O	Description	Pin Name	I/O	Description
1	RESERVED	/	/	PSM_IND*	DO	Power Supply Mode Indicator. 1.8V power domain.	RESERVED	/	/
2	RESERVED	/	/	ADC1	AI	ADC1 Input	RESERVED	/	/
4	PCM_CLK	DO	PCM data bit clock. 1.8V power domain.	I2S_BCLK*	DO	I2S bit clock. 1.8V power domain.	PCM_CLK	DO	PCM data bit clock. 1.8V power domain.
5	PCM_SYNC	DO	PCM data frame sync signal. 1.8V power domain.	I2S_WCLK*	DO	I2S data frame clock. 1.8V power domain.	PCM_SYNC	DO	PCM data frame sync signal. 1.8V power domain.
6	PCM_DIN	DI	PCM data input. 1.8V power domain.	I2S_D0*	IO	I2S data 0. 1.8V power domain.	PCM_DIN	DI	PCM data input. 1.8V power domain.
7	PCM_DOUT	DO	PCM data output. 1.8V power domain.	I2S_D1*	IO	I2S data 1. 1.8V power domain.	PCM_DOUT	DO	PCM data output. 1.8V power domain.
8	USB_VBUS	PI	USB insertion detection. 2.5V~5.25V.	USB_VBUS	PI	USB insertion detection. 2.5V~5.25V.	USB_VBUS	PI	USB insertion detection. 2.5V~5.25V.
9	USB_DP	IO	USB differential data bus (plus).	USB_DP	IO	USB differential data bus (plus).	USB_DP	IO	USB differential data bus (plus).
10	USB_DM	IO	USB differential data bus (minus).	USB_DM	IO	USB differential data bus (minus).	USB_DM	IO	USB differential data bus (minus).
15	PWRKEY	DI	Turn on the module. 1.8V power domain.	PWRKEY	DI	Turn on/off the module. 1.8V power domain.	PWRKEY	DI	Turn on/off the module. 1.8V power domain.

16	PWRDWN_N	DI	Turn off the module. Use it only when turning off the module via AT command failed. 1.8V power domain.	RESERVED	/	/	RESERVED	/	/
17	RESET_N	DI	Reset signal of the module. 1.8V power domain.	RESET_N	DI	Reset signal of the module. 1.8V power domain.	RESET_N	DI	Reset signal of the module. 1.8V power domain.
18	RESERVED	/	/	W_DISABLE#	DI	Airplane mode control. 1.8V power domain.	RESERVED	/	/
19	AP_READY*	DI	Application processor sleep state detection. 1.8V power domain.	AP_READY*	DI	Application processor sleep state detection. 1.8V power domain.	AP_READY*	DI	Application processor sleep state detection. 1.8V power domain.
20	STATUS	DO	Indicate the module's operation status.	STATUS	DO	Indicate the module's operation status.	STATUS	DO	Indicate the module's operation status.
21	NETLIGHT	DO	Indicate the module's network activity status.	NETLIGHT	DO	Indicate the module's network activity status.	NETLIGHT	DO	Indicate the module's network activity status.
22	RESERVED	/	/	DBG_RXD	DI	RXD of UART2 port. 1.8V power domain.	DBG_RXD	DI	RXD of debug UART. 1.8V power domain.
23	RESERVED	/	/	DBG_TXD	DO	TXD of UART2 port. 1.8V power domain.	DBG_TXD	DO	TXD of debug UART. 1.8V power domain.
24	RESERVED	/	/	ADC0	AI	ADC0 INPUT	RESERVED	/	/
25	CLK_OUT	DO	Provide a digital clock output for an	RESERVED	/	/	CLK_OUT	DO	Provide a digital clock output for an external

			external audio codec.						audio codec.
26	RESERVED	/	/	SPI_CLK*	DO	SPI master clock. 1.8V power domain.	SPI_CLK*	DO	SPI master clock. 1.8V power domain.
27	RESERVED	/	/	SPI_MOSI*	DO	Master Out Salve In of SPI interface. 1.8V power domain.	SPI_MOSI*	DO	Master Out Salve In of SPI interface. 1.8V power domain.
28	RESERVED	/	/	SPI_MISO*	DI	Master In Slave Out of SPI interface. 1.8V power domain.	SPI_MISO*	DI	Master In Slave Out of SPI interface. 1.8V power domain.
29	VDD_EXT	PO	Provide 1.8V for external circuit.	VDD_EXT	PO	Provide 1.8V for external circuit.	VDD_EXT	PO	Provide 1.8V for external circuit.
30	DTR	DI	Data terminal ready. Sleep mode control. 1.8V power domain.	DTR	DI	Data terminal ready. Sleep mode control. 1.8V power domain.	DTR	DI	Data terminal ready. Sleep mode control. 1.8V power domain.
32	VBAT_BB	PI	Power supply for module baseband part.	VBAT_BB	PI	Power supply for module baseband part.	VBAT_BB	PI	Power supply for module baseband part.
33	VBAT_BB	PI	Power supply for module baseband part.	VBAT_BB	PI	Power supply for module baseband part.	VBAT_BB	PI	Power supply for module baseband part.
34	RXD	DI	Receive data. 1.8V power domain.	RXD	DI	Receive data. 1.8V power domain.	RXD	DI	Receive data. 1.8V power domain.
35	TXD	DO	Transmit data. 1.8V power domain.	TXD	DO	Transmit data. 1.8V power domain.	TXD	DO	Transmit data. 1.8V power domain.
36	CTS	DO	Clear to send. 1.8V power domain.	CTS	DO	Clear to send. 1.8V power domain.	CTS	DO	Clear to send. 1.8V power domain.
37	RTS	DI	Request to send. 1.8V power domain.	RTS	DI	Request to send. 1.8V power domain.	RTS	DI	Request to send. 1.8V power domain.

38	DCD	DO	Data carrier detection. 1.8V power domain.	DCD	DO	Data carrier detection. 1.8V power domain.	DCD	DO	Data carrier detection. 1.8V power domain.
39	RI	DO	Ring indictor. 1.8V power domain.	RI	DO	Ring indictor. 1.8V power domain.	RI	DO	Ring indictor. 1.8V power domain.
40	I2C_SCL	OD	I2C serial clock. 1.8V power domain.	I2C_SCL	OD	I2C serial clock. 1.8V power domain.	I2C_SCL	OD	I2C serial clock. 1.8V power domain.
41	I2C_SDA	OD	I2C serial data. 1.8V power domain.	I2C_SDA	OD	I2C serial data. 1.8V power domain.	I2C_SDA	OD	I2C serial data. 1.8V power domain.
42	USIM_ PRESENCE	DI	(U)SIM card insertion detection. 1.8V power domain.	USIM_ PRESENCE	DI	(U)SIM card insertion detection. 1.8V power domain.	USIM1_ PRESENCE	DI	(U)SIM1 card insertion detection. 1.8V power domain.
43	USIM_VDD	PO	Power supply for (U)SIM card. 1.8V/3.0V	USIM_VDD	PO	Power supply for (U)SIM card. 1.8V/3.0V	USIM1_VDD	PO	Power supply for (U)SIM1 card. 1.8V/3.0V
44	USIM_RST	DO	Reset signal of (U)SIM card. 1.8V/3.0V	USIM_RST	DO	Reset signal of (U)SIM card. 1.8V/3.0V	USIM1_RST	DO	Reset signal of (U)SIM1 card. 1.8V/3.0V
45	USIM_DATA	IO	Data signal of (U)SIM card. 1.8V/3.0V	USIM_DATA	IO	Data signal of (U)SIM card. 1.8V/3.0V	USIM1_DATA	IO	Data signal of (U)SIM1 card. 1.8V/3.0V
46	USIM_CLK	DO	Clock signal of (U)SIM card. 1.8V/3.0V	USIM_CLK	DO	Clock signal of (U)SIM card. 1.8V/3.0V	USIM1_CLK	DO	Clock signal of (U)SIM1 card. 1.8V/3.0V
47	USIM_GND	/	Specified ground for (U)SIM card.	USIM_GND	/	Specified ground for (U)SIM card.	USIM_GND	/	Specified ground for (U)SIM card.
49	RESERVED	/	/	ANT_GNSS	AI	GNSS antenna interface.	ANT_DIV	AI	Diversity antenna interface.
51	VRTC	PI/	VO=1.8V	RESERVED	/	/	RESERVED	/	/

		PO	VI=1.0V~1.9V I_{IN} max=2uA when VBAT is not applied.						
52	VBAT_RF	PI	Power supply for module RF part.	VBAT_RF	PI	Power supply for module RF part.	VBAT_RF	PI	Power supply for module RF part.
53	VBAT_RF	PI	Power supply for module RF part.	VBAT_RF	PI	Power supply for module RF part.	VBAT_RF	PI	Power supply for module RF part.
60	RF_ANT	IO	RF antenna interface.	ANT_MAIN	IO	RF antenna interface.	ANT_MAIN	IO	RF antenna interface.
63	RESERVED	/	/	I2S_MCLK*	DO	I2S master clock. 1.8V power domain.	RESERVED	/	/
64	RESERVED	/	/	GPIO*	IO	General-purpose input/output. 1.8V power domain.	RESERVED	/	/
75	RESERVED	/	/	USB_BOOT	DI	Force the module to boot from USB port. 1.8V power domain.	USB_BOOT	DI	Force the module to boot from USB port. 1.8V power domain.
83	RESERVED	/	/	RESERVED	/	/	USIM2_ PRESENCE	DI	(U)SIM2 card insertion detection. 1.8V power domain.
84	RESERVED	/	/	RESERVED	/	/	USIM2_CLK	DO	Clock signal of (U)SIM2 card. 1.8V/3.0V.
85	RESERVED	/	/	RESERVED	/	/	USIM2_RST	DO	Reset signal of (U)SIM2 card. 1.8V/3.0V.
86	RESERVED	/	/	RESERVED	/	/	USIM2_ DATA	IO	Data signal of (U)SIM2 card. 1.8V/3.0V.

87	RESERVED	/	/	RESERVED	/	/	USIM2_VDD	PO	Power supply for (U)SIM2 card. 1.8V/3.0V.
3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67~74, 79~82, 89~91, 100~102	GND	/	Ground	GND	/	Ground	GND	/	Ground
11~14, 56, 57, 65~66, 76~78, 88, 92~99	RESERVED	/	/	RESERVED	/	/	RESERVED	/	/

NOTES

1. The green and orange colored pins are different functional pins between EG9x and BG96.
2. The green and purple colored pins are different functional pins between EG9x and UG96/UG95.
3. The other pins are compatible pins with the same functions.
4. Keep all reserved and unused pins unconnected.
5. All GND pins should be connected to ground.
6. “*” means under development.

4 Hardware Reference Design

The following chapters describe the compatible design among EG9x, BG96, UG96 and UG95 on main functionalities.

4.1. Power Supply

4.1.1. Reference Design for Power Supply

Power design for a module is very important, as the performance of a module largely depends on the power source. The power supply for EG9x, BG96, UG96 and UG95 should be able to provide sufficient current up to 2A. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for these modules. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source. The typical output of the power supply is about 3.8V and the maximum load current is 3A.

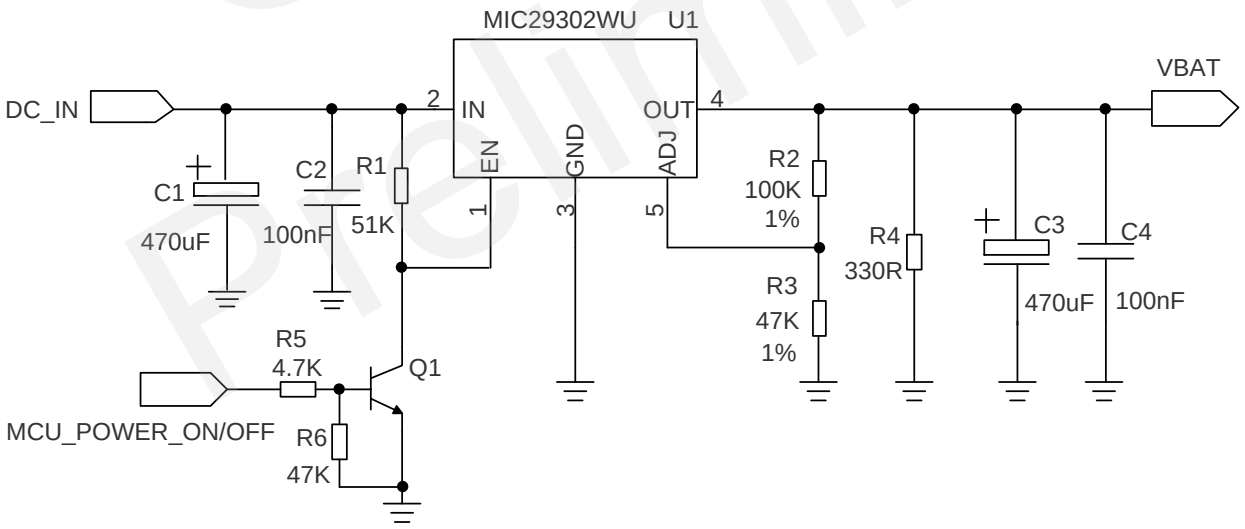

Figure 2: Reference Circuit of Power Supply

4.1.2. Reduce Voltage Drop

The power supply range of EG9x/BG96/UG96/UG95 is from 3.3V to 4.3V. Attention should be paid to the range of the power source to make sure that the input voltage will never drop below 3.3V and never exceed 4.3V, and the typical power supply is 3.8V. The VBAT to EG9x/BG96/UG96/UG95's VBAT_BB and VBAT_RF pins should be divided into two separated paths in star structure. In addition, in order to get a stable output voltage, it is suggested to use a zener diode whose reverse zener voltage is 5.1V and dissipation power is above 0.5 watt.

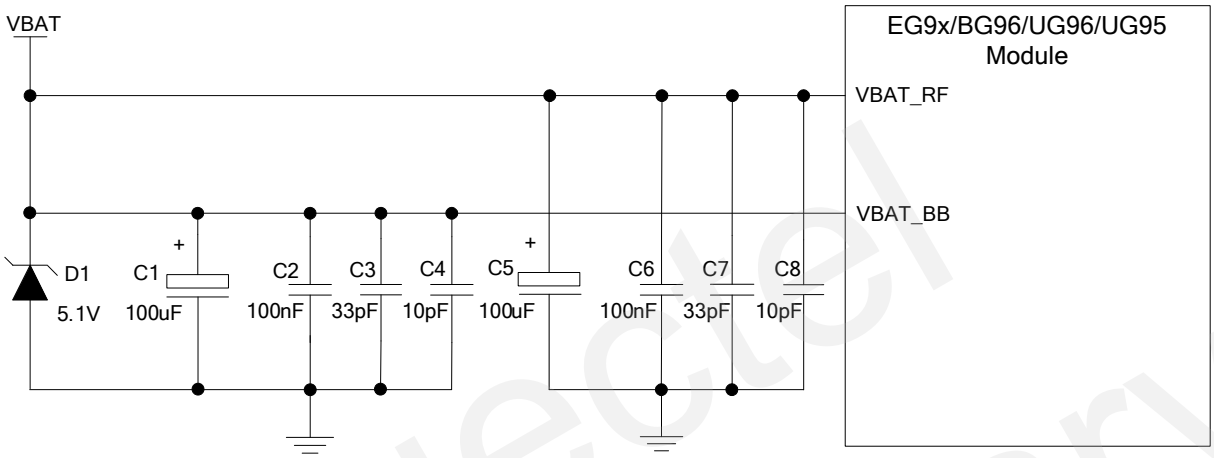

Figure 3: Reference Circuit of VBAT

4.2. Power-on Circuit

The turn-on method of EG9x is the same as BG96/UG96/UG95, and EG9x/BG96/UG96/UG95 will be powered on after pressing PWRKEY for a certain time.

The following is a reference design for the power-on circuit of UG96/UG95. EG9x/BG96 can also be powered on or off via this circuit, though the power domain of its PWRKEY is different from that of UG96/UG95.

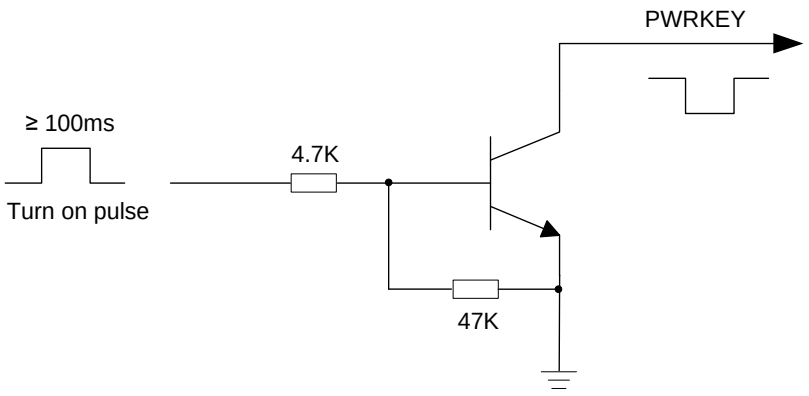

Figure 4: Driving Circuit of the PWRKEY

The turning on scenarios of EG9x, BG96, UG96 and UG95 are illustrated in the figure below.

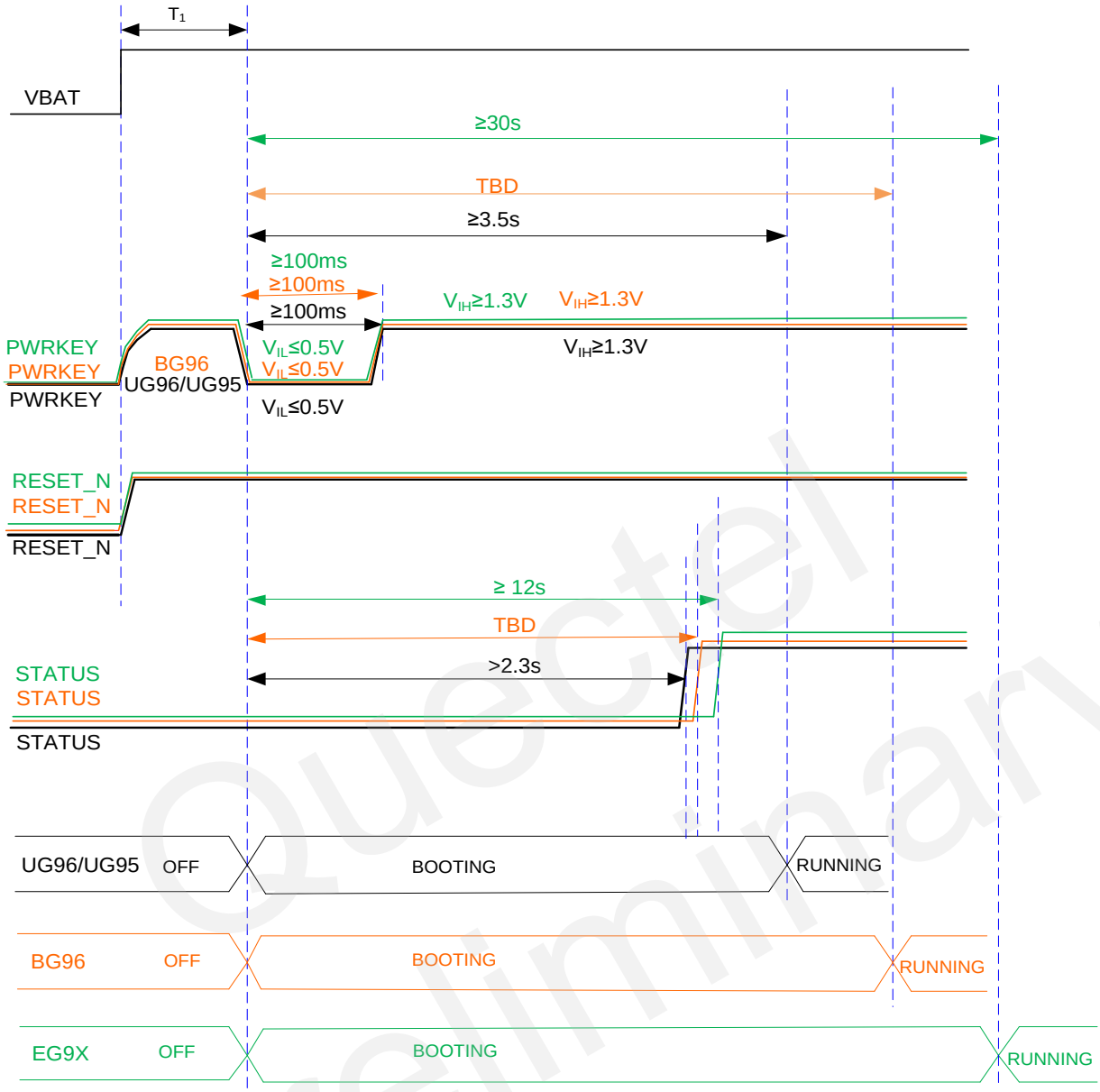

Figure 5: Timing of Turning on Scenarios

NOTES

1. Please make sure VBAT is stable before pulling down PWRKEY pin. The time of T_1 is recommended to be 100ms. It is not recommended to always pull down PWRKEY pin.
2. The parts marked in green in the above figure are for EG9x.
3. The parts marked in orange in the above figure are for BG96.
4. The parts marked in black in the above figure are for UG96 and UG95.

4.3. Power-off Circuit

4.3.1. Power down Module via AT Command

There are several ways to turn off EG9x/BG96/UG96/UG95 module. It is recommended to turn off the module through **AT+QPOWD** command. It is a safe way to turn off the module. This command will let the module log out from the network and allow the firmware to save important data before completely disconnecting the power supply.

The power-down scenario of EG9x/BG96/UG96/UG95 is illustrated in the figure below.

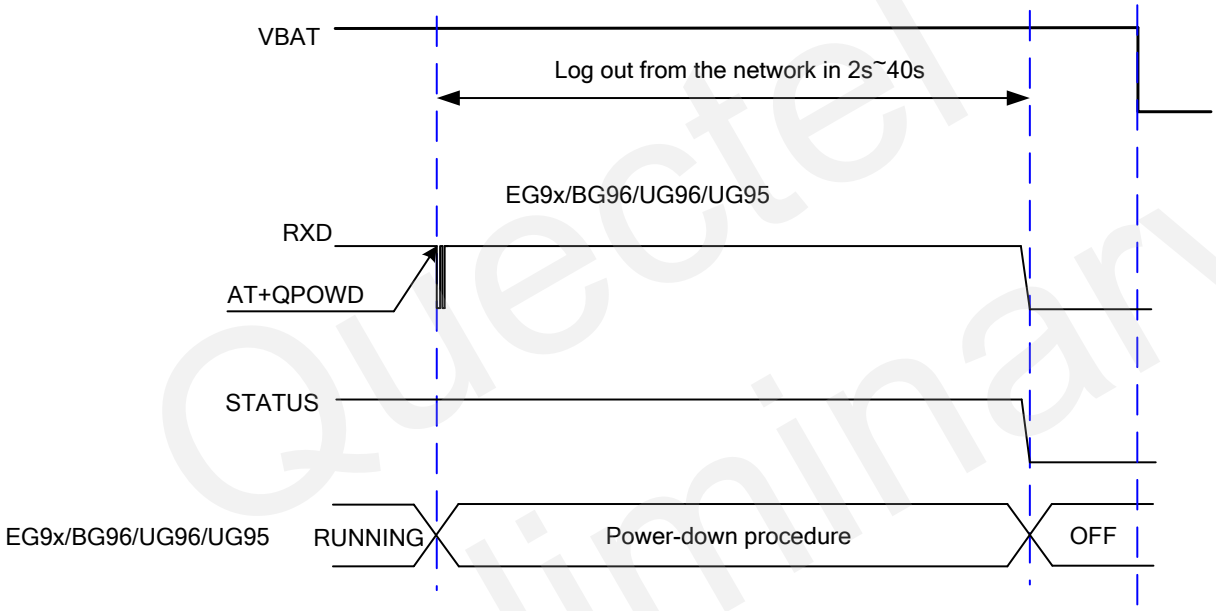

Figure 6: Timing of Turning off through AT Command

NOTE

The time for the module to log out from network depends on local network quality.

4.3.2. Emergency Shutdown for UG96/UG95

UG96/UG95 module can be shut down by PWRDWN_N pin, while EG9x and BG96 do not have this pin. This pin should only be used under emergent situations. Although turning off the module by PWRDWN_N is fully tested and nothing wrong detected, this operation is still a big risk as it could reduce the service life of (U)SIM card or the module.

The following circuit is a reference design for the emergency shutdown circuit of UG96/UG95.

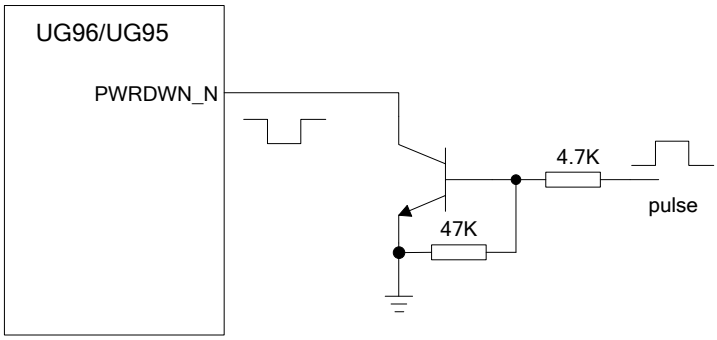

Figure 7: Driving Circuit of Emergency Shutdown Circuit (for UG96/UG95 Only)

The emergency shutdown scenario is illustrated in the figure below.

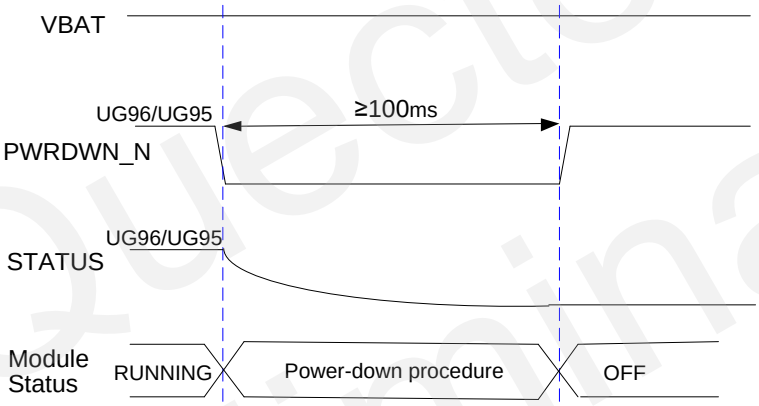

Figure 8: Timing of Emergency Shutdown (for UG96/UG95 Only)

4.3.3. Power down EG9x/BG96 Using PWRKEY Pin

It is a safe way to turn off EG9x/BG96 module by driving PWRKEY to a low level voltage for a certain time, while UG96/UG95 could not be turned off by this pin.

The power-down scenario for EG9x/BG96 by PWRKEY is illustrated in the figure below.

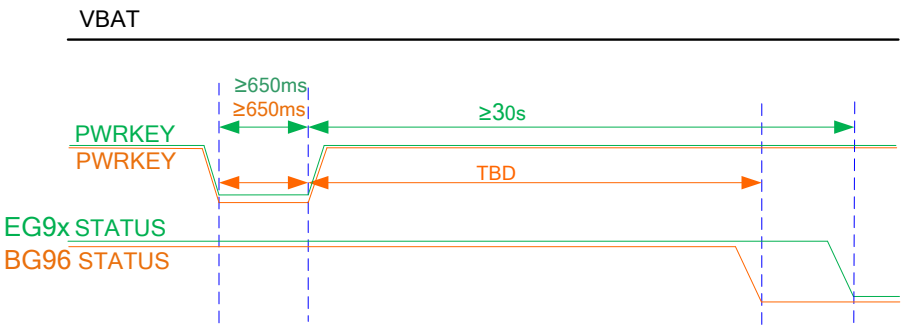

Figure 9: Timing of Turning off EG9x/BG96 by PWRKEY

NOTES

1. The parts marked in green in the above figure are for EG9x.
2. The parts marked in orange in the above figure are for BG96.

4.4. Reset the Module

EG9x/BG96/UG96/UG95 module can be reset by RESET_N pin. The modules can be reset by driving RESET_N to a low level voltage for some time.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control RESET_N.

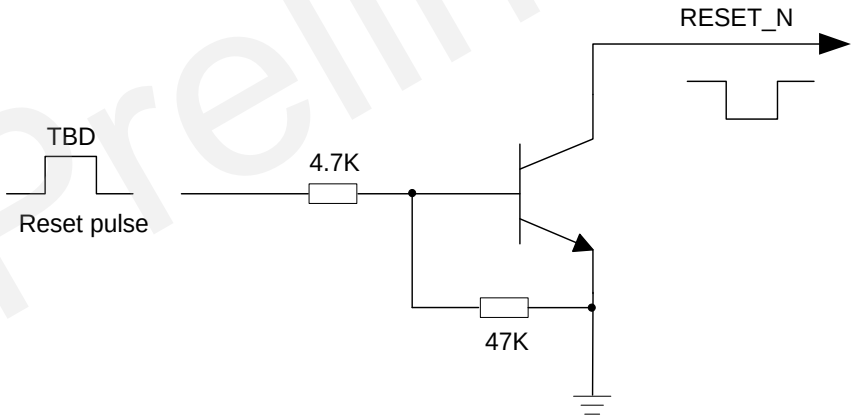

Figure 10: Reference Circuit of RESET_N by Using Driving Circuit

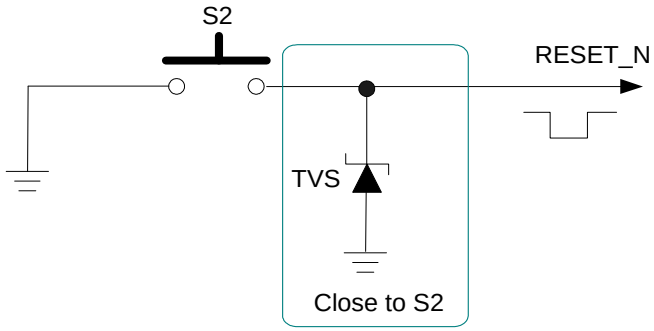

Figure 11: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the figure below.

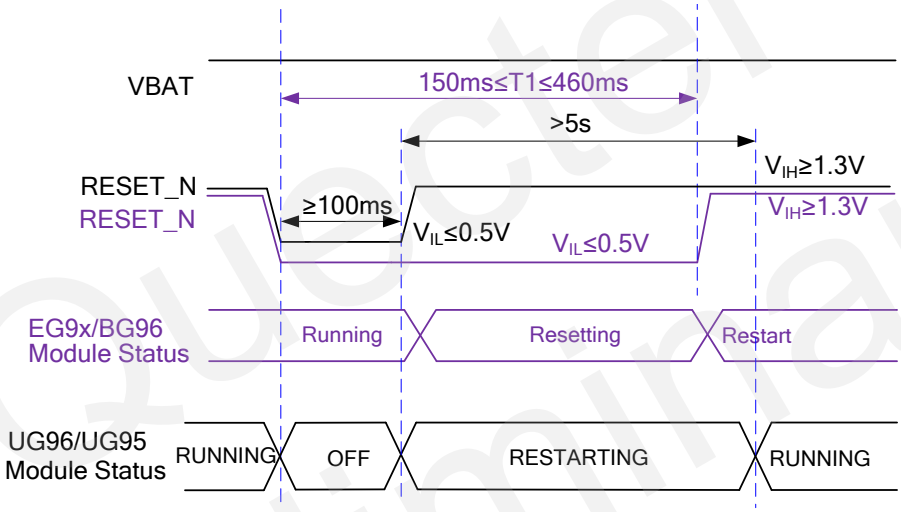

Figure 12: Timing of Resetting Module

NOTES

1. Use the RESET_N only when turning off the module by **AT+QPOWD** command and PWRKEY pin both failed.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.
3. The parts marked in purple in the above figure are for EG9x and BG96.
4. The parts marked in black in the above figure are for UG96 and UG95.

4.5. Network Status Indication

The NETLIGHT pin can be used to drive a network status indicator LED. A reference design is shown below.

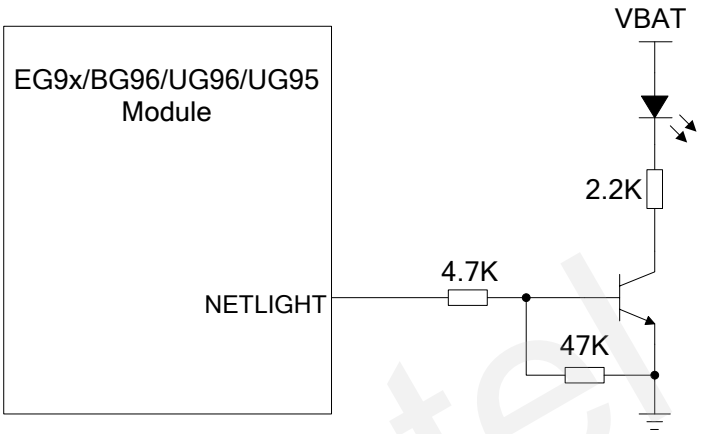

Figure 13: Reference Circuit of NETLIGHT

4.6. Operation Status Indication

The STATUS pin is used to indicate EG9x/BG96/UG96/UG95's operation status. It will output high level when the module is powered on. The following figure shows a reference circuit for STATUS.

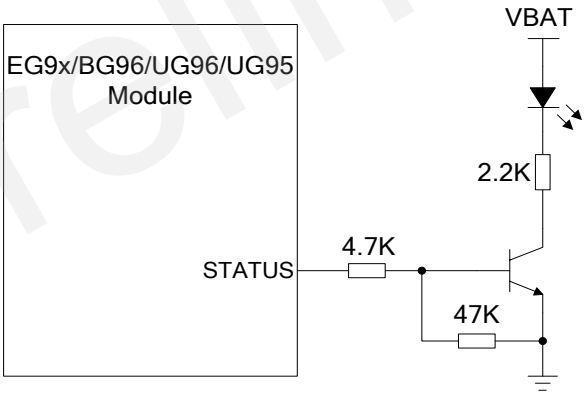

Figure 14: Reference Circuit of STATUS

4.7. (U)SIM Card Interface

(U)SIM card interface of EG9x/BG96/UG96/UG95 supports 1.8V or 3.0V (U)SIM cards. The pin assignment of EG9x's (U)SIM1/(U)SIM2 card interface and BG96/UG96/UG95's (U)SIM card interface are compatible among each other.

The following figure shows a reference design for (U)SIM card interface with a 6-pin (U)SIM card connector.

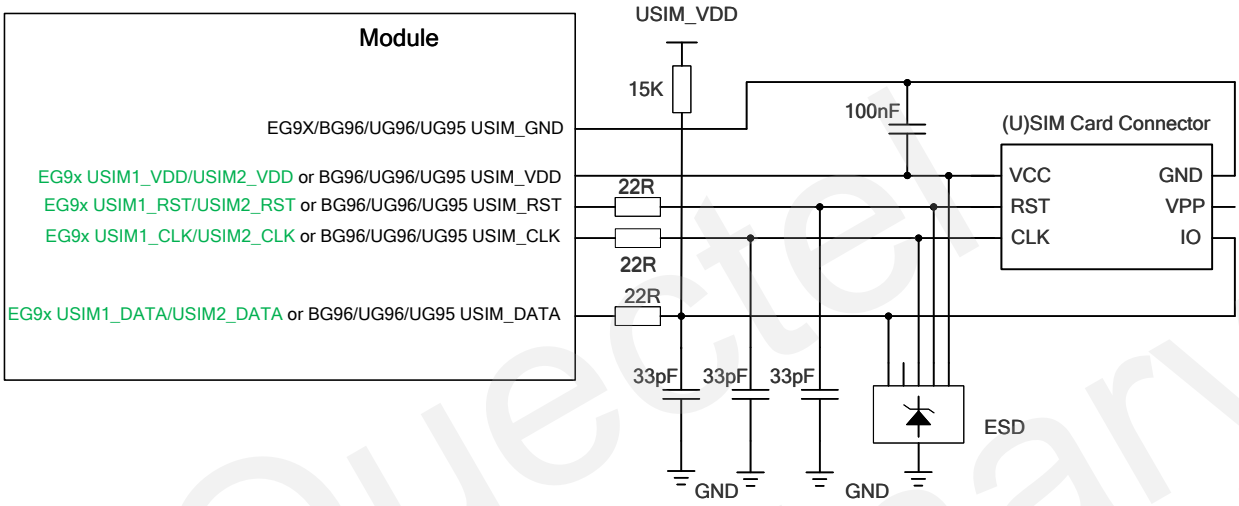

Figure 15: Reference Circuit of (U)SIM Card Interface with a 6-Pin (U)SIM Card Connector

If (U)SIM card detection function is used, keep USIM_PRESENCE pin connected. The following figure shows a reference design for (U)SIM card interface with (U)SIM card detection function.

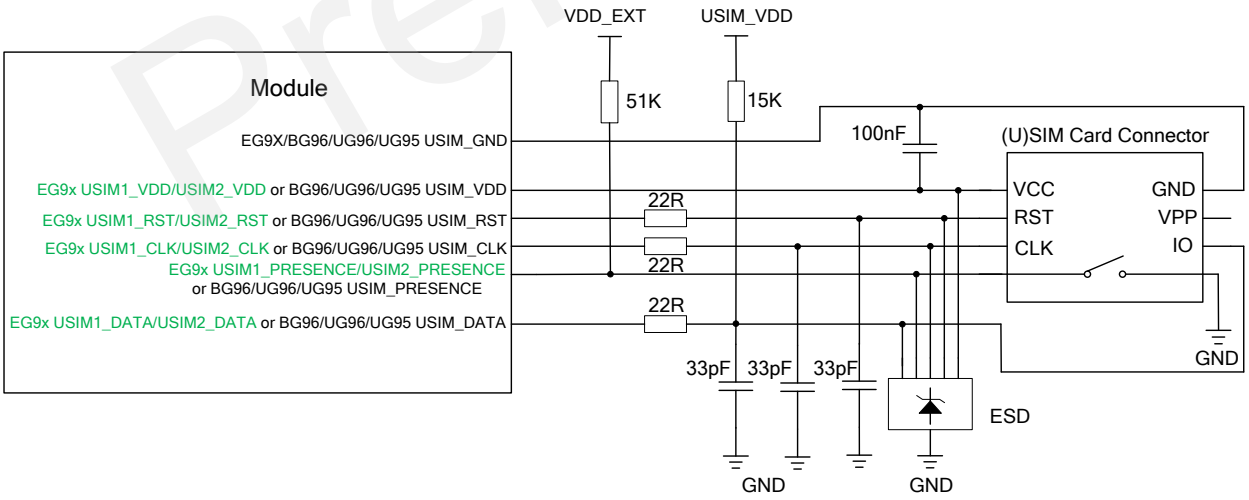

Figure 16: Reference Design of of (U)SIM Card Interface with (U)SIM Card Detection

NOTES

1. The green colored pin names are for EG9x only.
2. EG9x has two (U)SIM card interfaces, either of which is compatible with the (U)SIM card interface of BG96/UG96/UG95.

4.8. Serial Interfaces

EG9x/BG96/UG96/UG95 can communicate with application processor via USB interface or UART interface. It is recommended to choose the right communication mode for customers' designs.

4.8.1. UART Interface

The following is a reference design of the main UART interface, when the application processor communicates with EG9x/BG96/UG96/UG95 via UART interface. It is recommended to add a level match circuit between the module and the MCU, because of the different power domain of their UART interface. For details, please refer to ***document [1]***, ***[2]***, ***[3]***, ***[4]*** and ***[5]***.

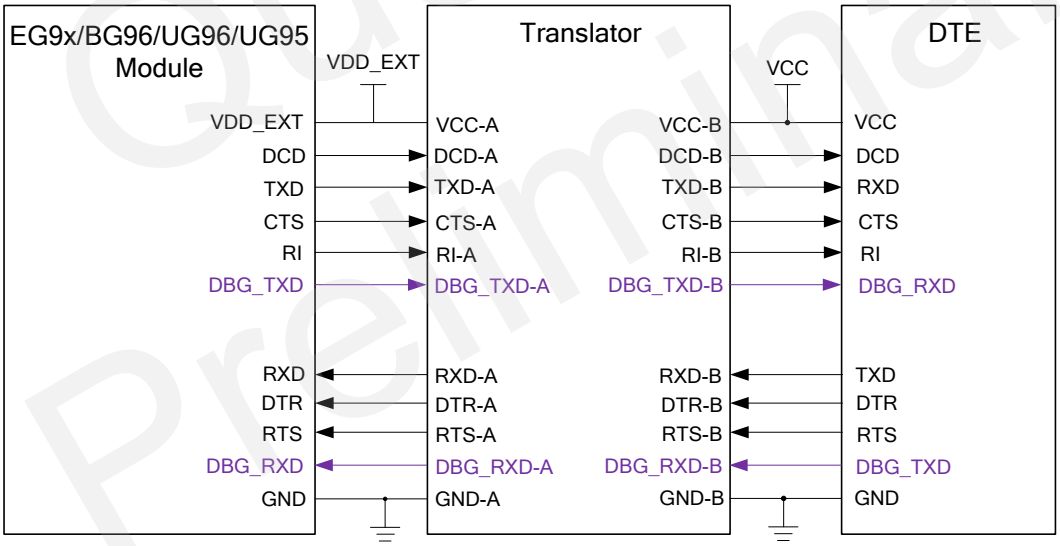

Figure 17: Reference Design of UART Interface

NOTES

1. UART pins of EG9x/BG96/UG96/UG95 belong to 1.8V power domain.
2. The parts marked in purple in the above figure are for EG9x's debug UART and BG96's UART2.

4.8.2. USB Interface

EG9x/BG96/UG96/UG95 contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high speed (480Mbps) and full speed (12Mbps) modes. The interface supports USB devices only.

The following shows a reference design of USB interface, when the application processor communicates with EG9x/BG96/UG96/UG95 module via USB interface.

Please pay attention to the voltage level match between the module and the processor. For details, please refer to ***document [1]***, ***[2]***, ***[3]***, ***[4]*** and ***[5]***.

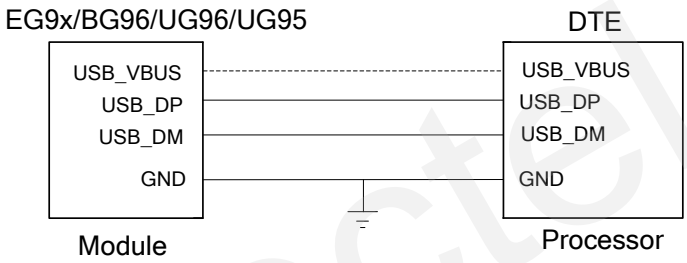

Figure 18: Reference Design of USB Interface

NOTE

It is recommended to reserve USB_DP, USB_DM and USB_VBUS pins as test points and place these test points on the DTE for debugging.

4.9. Audio Interfaces

EG9x/BG96/UG96/UG95 module provides a PCM audio interface.

The following shows a reference compatible design for the PCM interface of EG9x/BG96/UG96/UG95. For more details, please refer to ***document [1]***, ***[2]***, ***[3]***, ***[4]*** and ***[5]***.

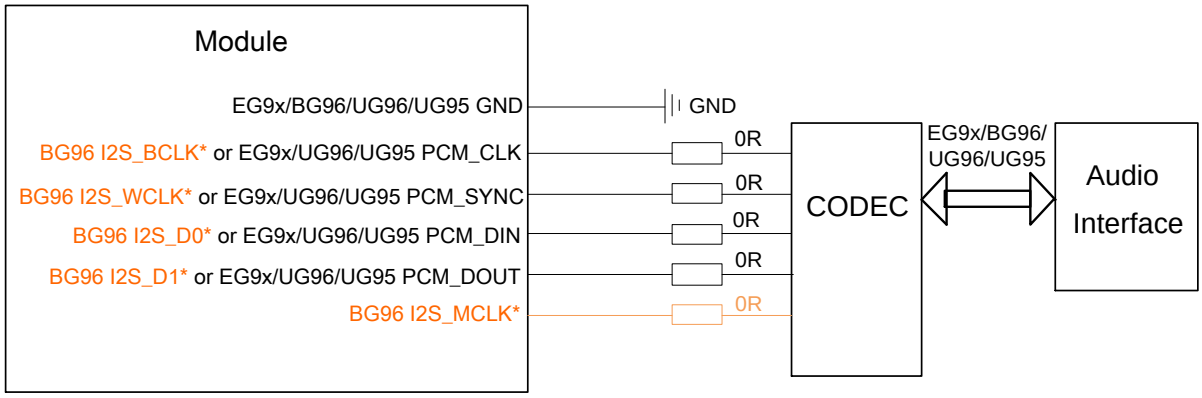

Figure 19: Reference Design of Audio Interface

NOTES

1. The parks marked in orange in the above figure are for BG96 only.
2. For more details about the PCM interface configuration of UG96 and UG95, please refer to the **AT+QDAC** command in ***document [9]***.

4.10. Antenna Interfaces

The pin assignment of EG9x/BG96's ANT_MAIN and UG96/UG95's RF_ANT are compatible among each other. ANT_DIV is unique to EG9x. The main/RF antenna interface has an impedance of 50Ω. A reference circuit is shown below. In order to achieve better RF performance, a π-type matching circuit should be reserved, and the π-type matching components (R1/C1/C2, R2/C3/C4) should be placed as close to the antennas as possible. By default, the resistance of R1/R2 is 0Ω and capacitors C1/C2/C3/C4 are not mounted.

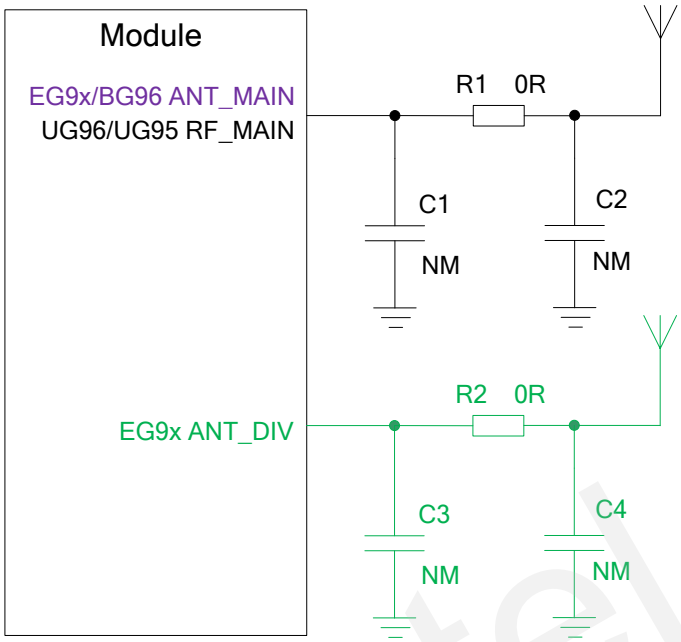

Figure 20: Reference Circuit of RF Interface

NOTE

The parts marked in green in the above figure are for EG9x only.

EG9x/UG96/UG95 does not have ANT_GNSS antenna interface. A reference design for ANT_GNSS antenna interface of BG96 is shown as below.

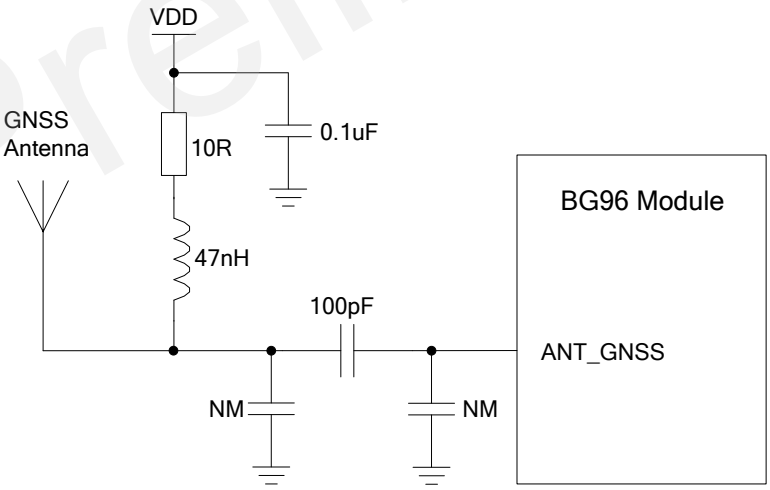

Figure 21: Reference Circuit of BG96 ANT_GNSS Interface

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If BG96 module is designed with a passive antenna, then the VDD circuit is not needed.

5 Recommended Footprint

The following figure shows the bottom view of EG9x, BG96, UG96 and UG95.

Figure 22: Bottom View of EG9x/BG96/UG96/UG95

The following figure shows the recommended compatible footprint of EG9x, BG96, UG96 and UG95.

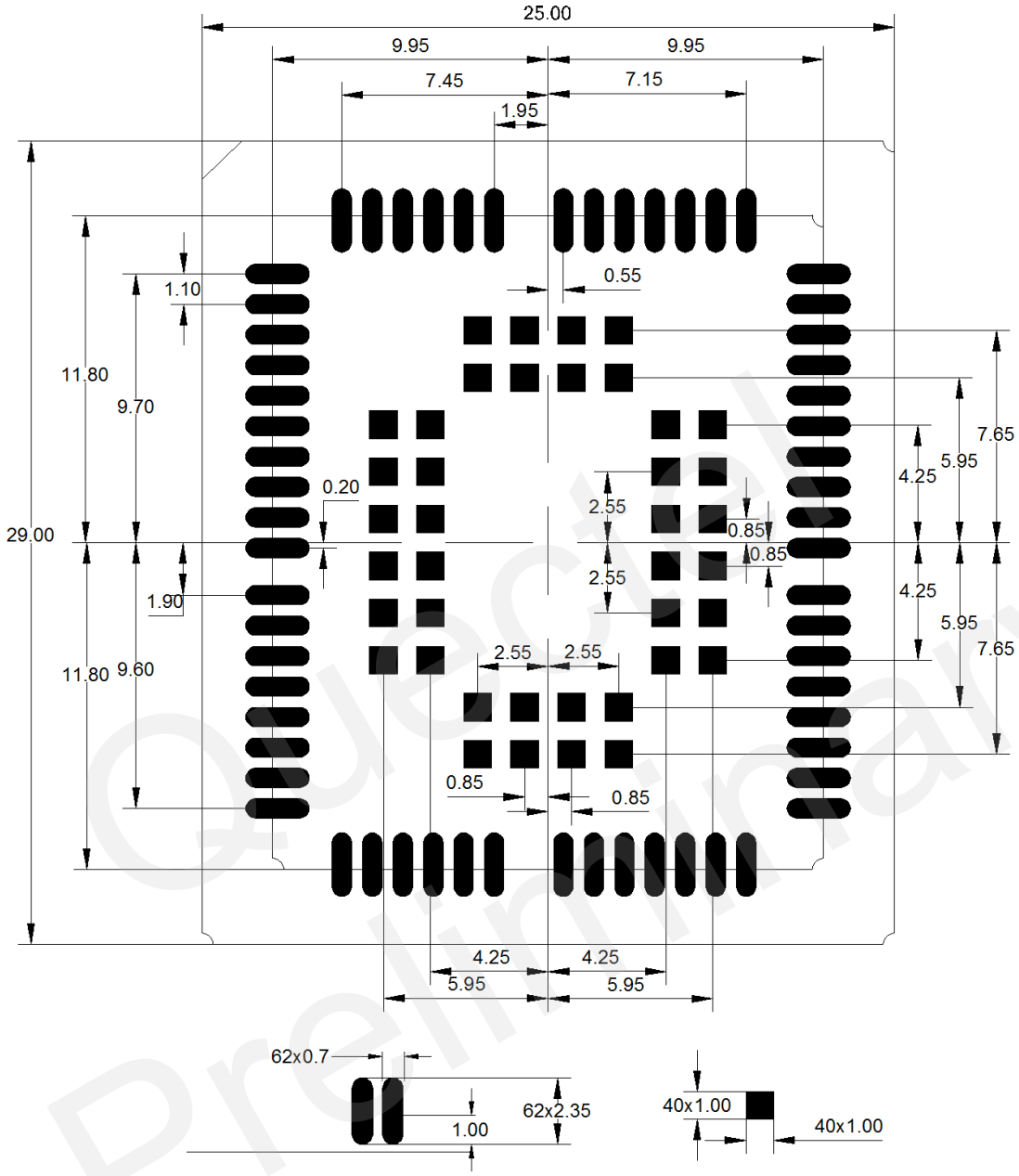

Figure 23: Recommended Footprint of EG9x/BG96/UG96/UG95 (Unit: mm)

The thickness of PCB is different. In order to ensure the module soldering quality, the thickness of stencil is recommended to be 0.13mm for UG96/UG95 and 0.18mm for EG9x/BG96. For more details, please refer to ***document [6]***.

The recommended stencil design for EG9x is shown as below.

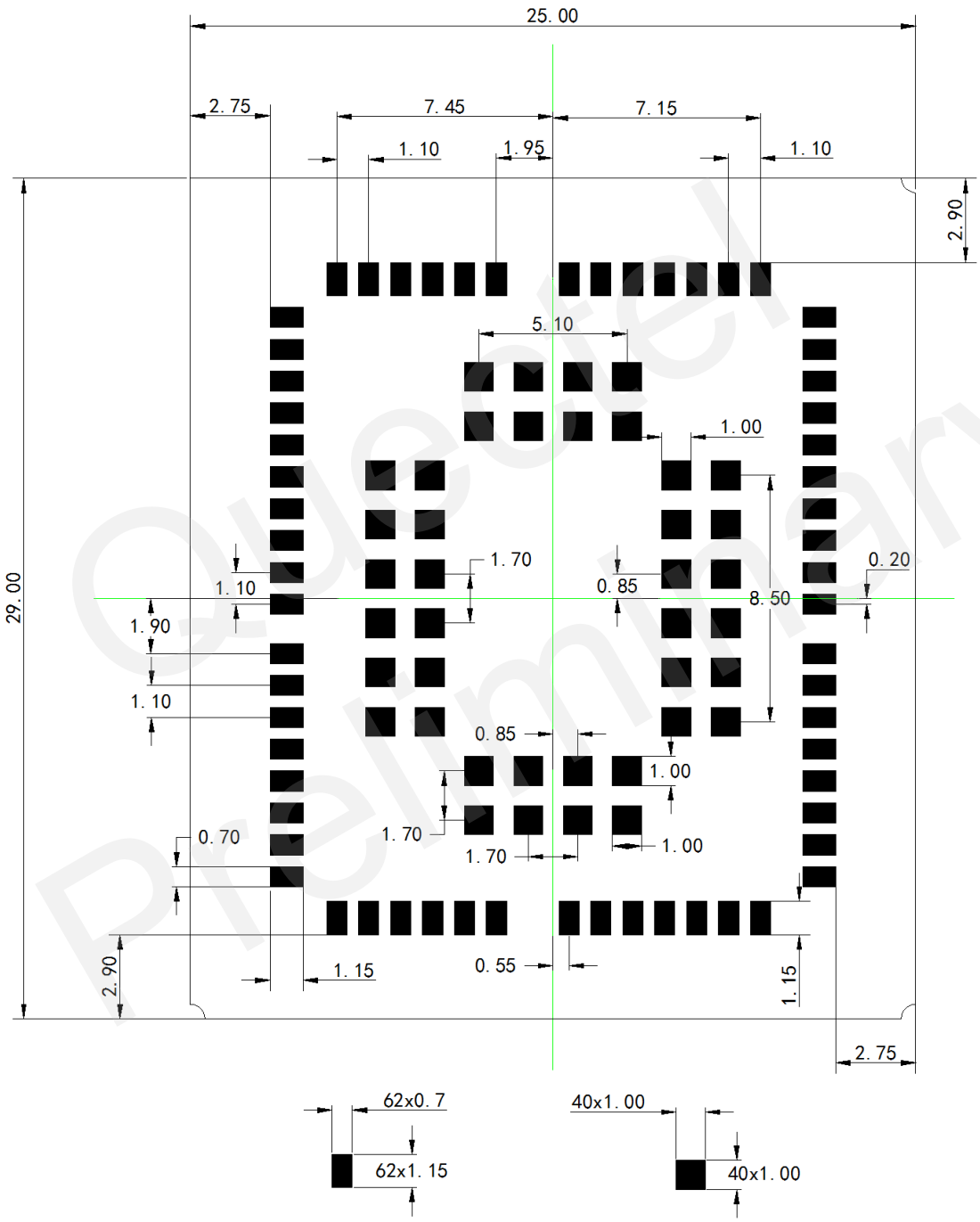

Figure 24: Recommended Stencil Design for EG9x (Unit: mm)

The recommended stencil design for BG96/UG96 is shown as below.

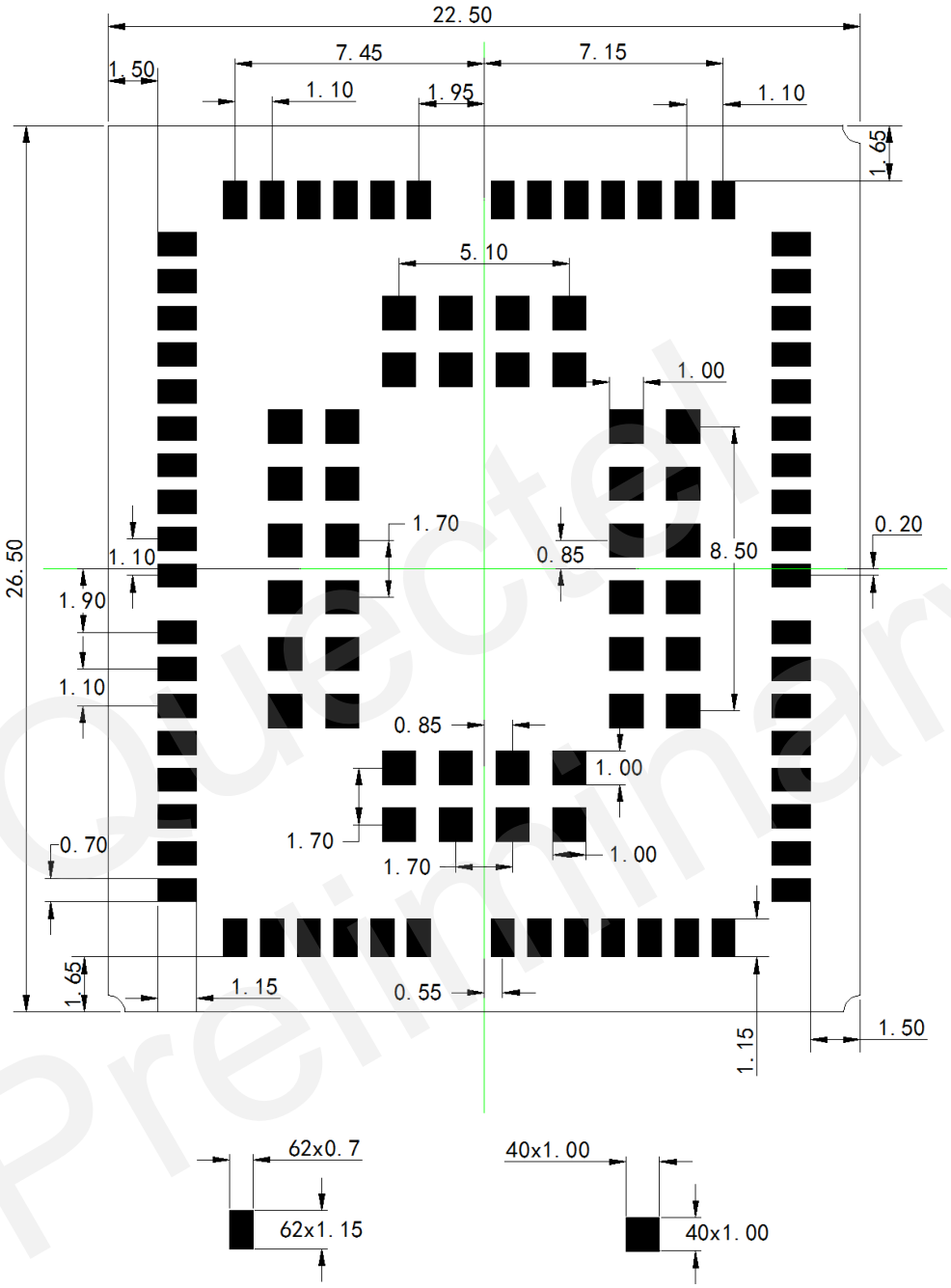

Figure 25: Recommended Stencil Design for BG96/UG96 (Unit: mm)

The recommended stencil design for UG95 is shown as below.

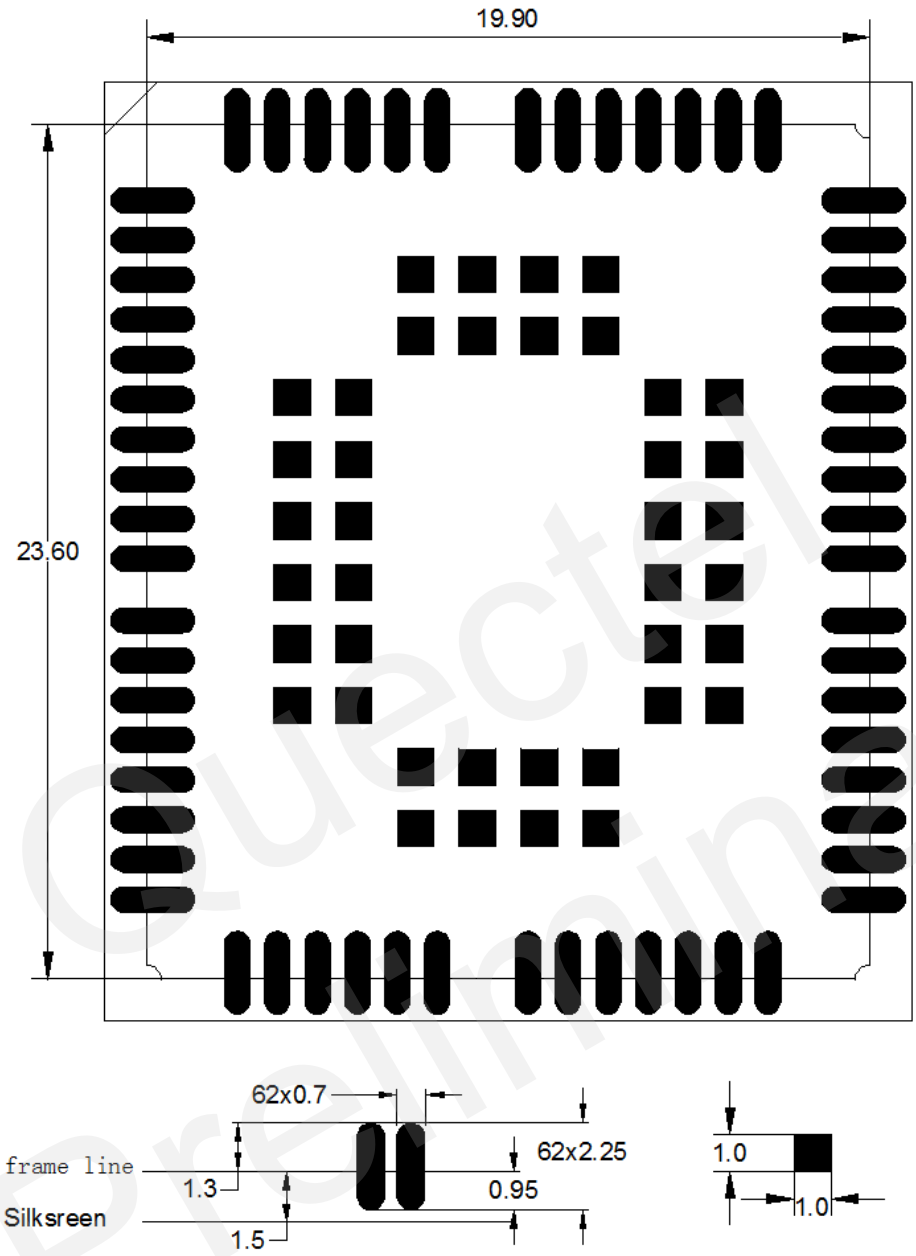

Figure 26: Recommended Stencil Design for UG95 (Unit: mm)

The following figure shows the sketch map of installation for EG9x, BG96, UG96 and UG95.

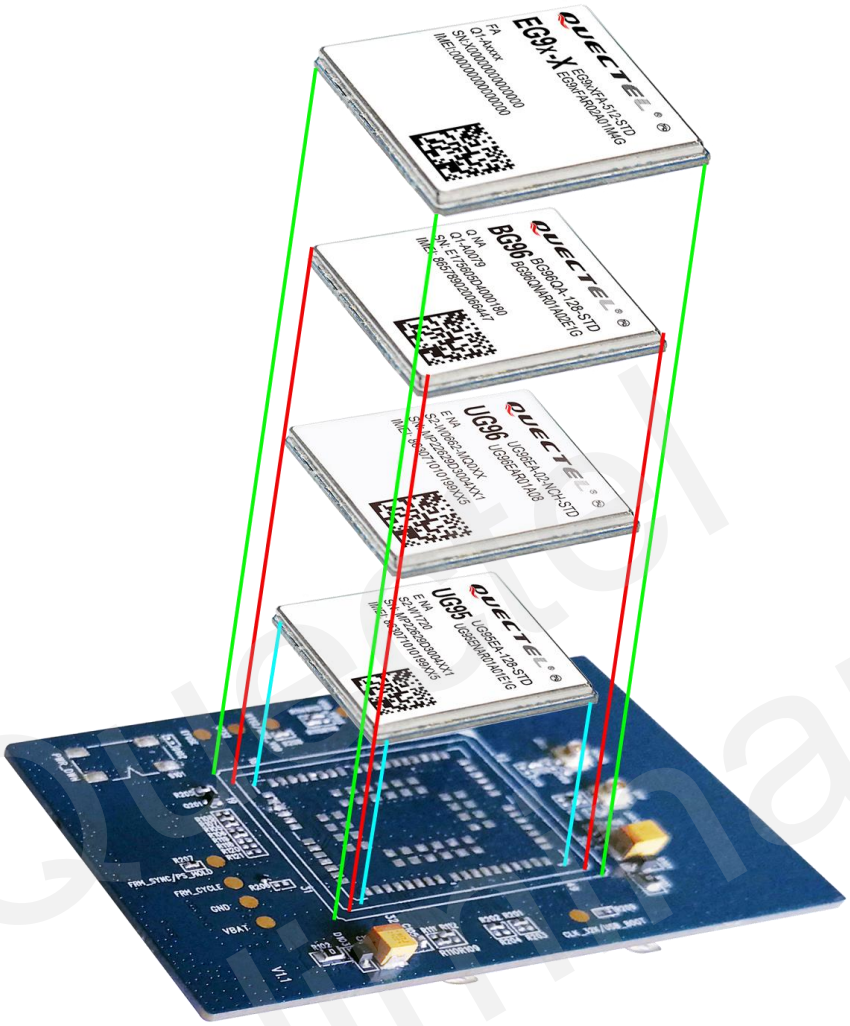

Figure 27: Installation Sketch Map for EG9x/BG96/UG96/UG95

6 Manufacturing and Packaging

6.1. Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass.

It is suggested that the peak reflow temperature is 235~245ºC (for SnAg3.0Cu0.5 alloy). The absolute max reflow temperature is 260ºC. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below.

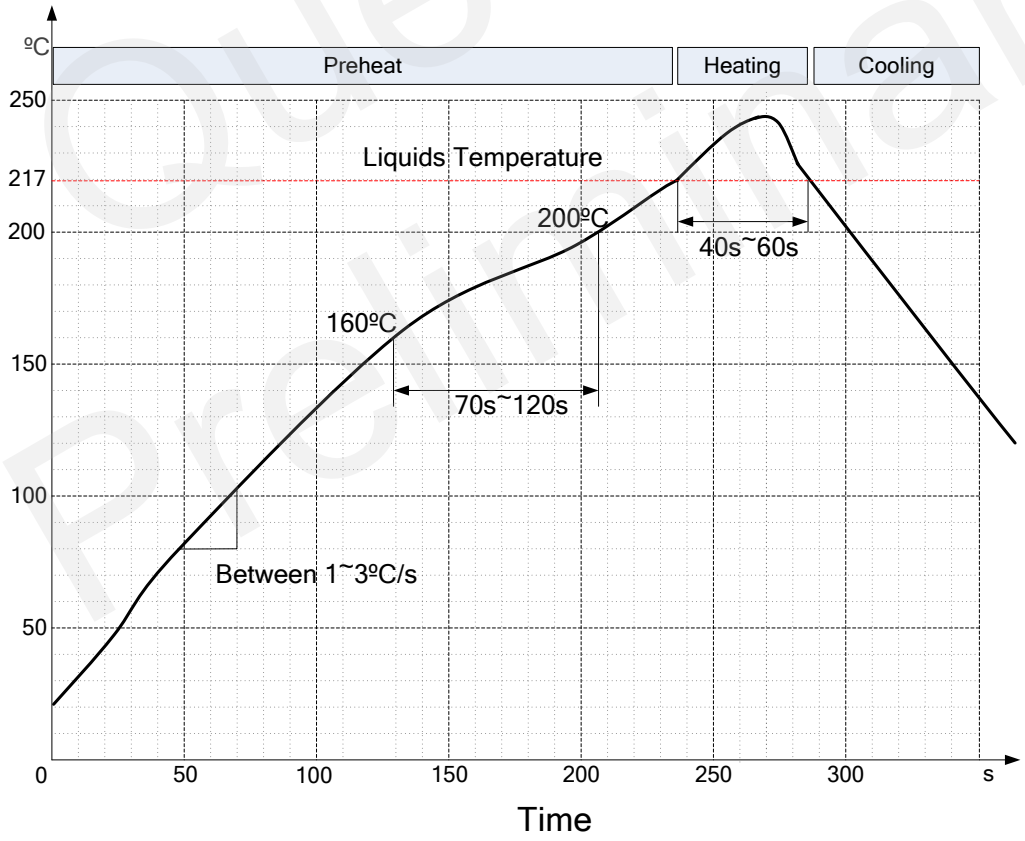

Figure 28: Reflow Soldering Thermal Profile

6.2. Packaging

The modules are stored inside a vacuum-sealed bag which is ESD protected. It should not be opened until the devices are ready to be soldered onto the application.

6.2.1. EG9x Packaging

Tape and reel dimensions of EG9x are TBD.

6.2.2. BG96/UG96 Packaging

The reel is 330mm in diameter and each reel contains 250 modules.

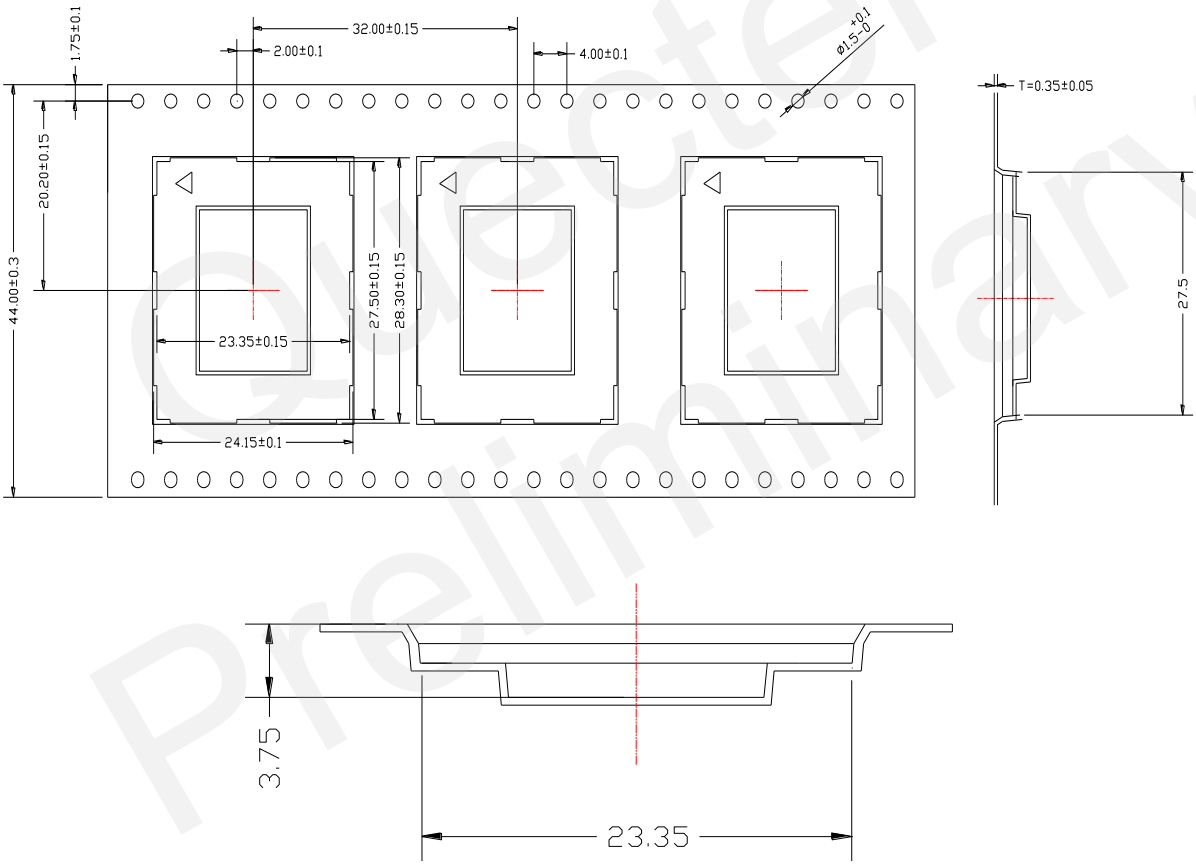

Figure 29: Tape Dimensions of BG96/UG96

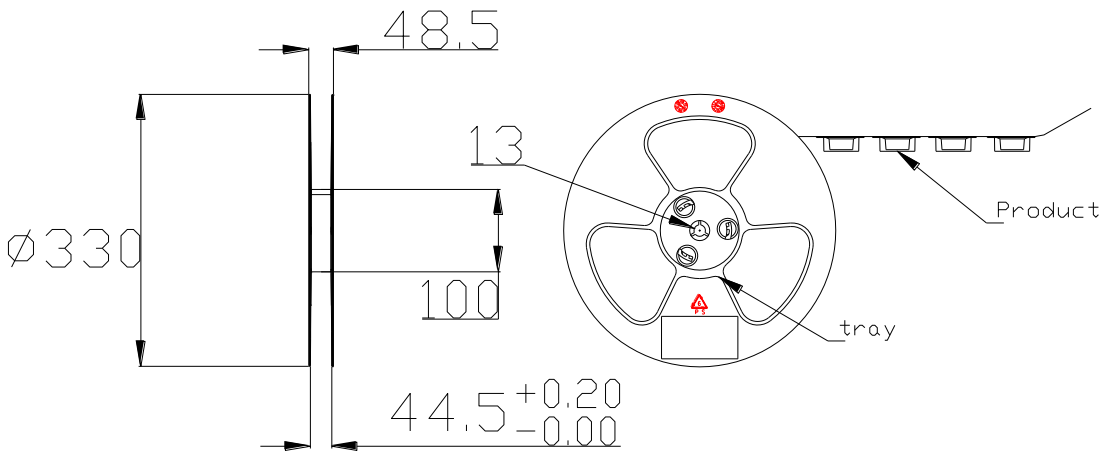

Figure 30: Reel Dimensions of BG96/UG96

6.2.3. UG95 Packaging

The reel is 330mm in diameter and each reel contains 250 modules.

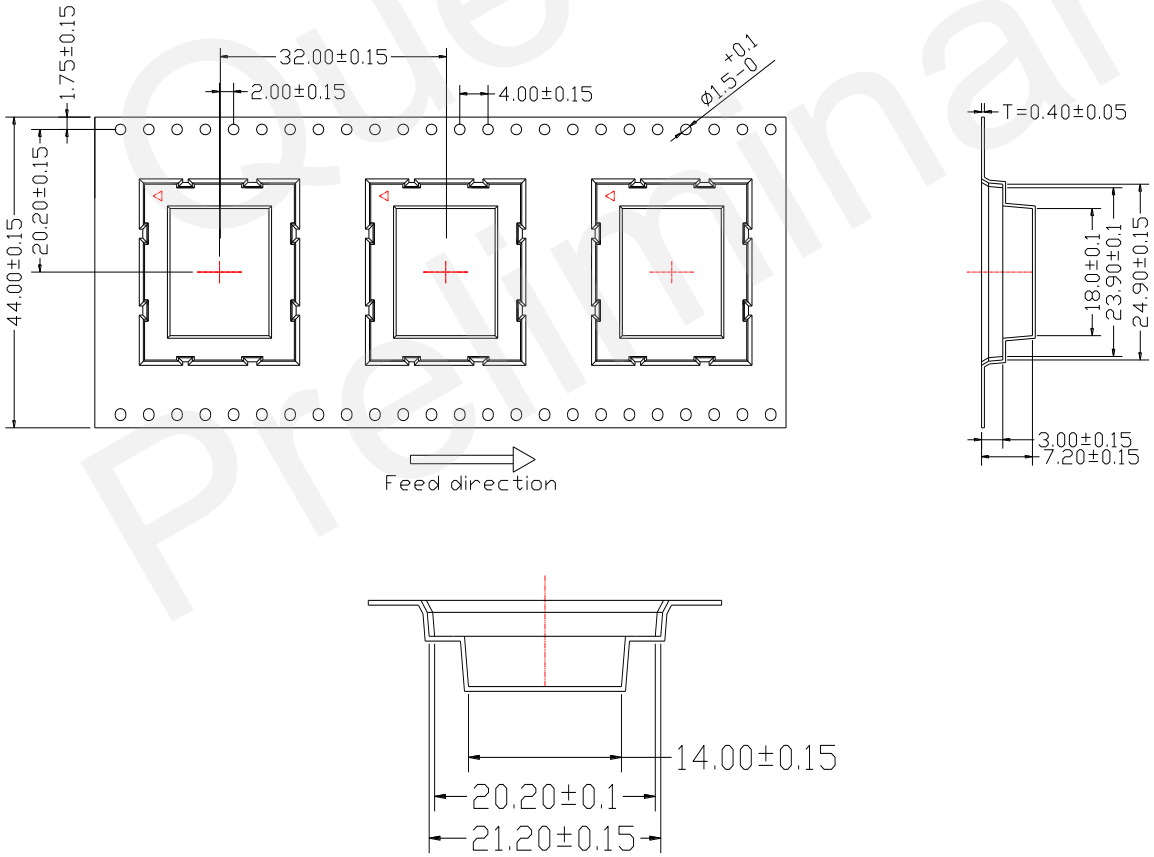

Figure 31: Tape Dimensions of UG95

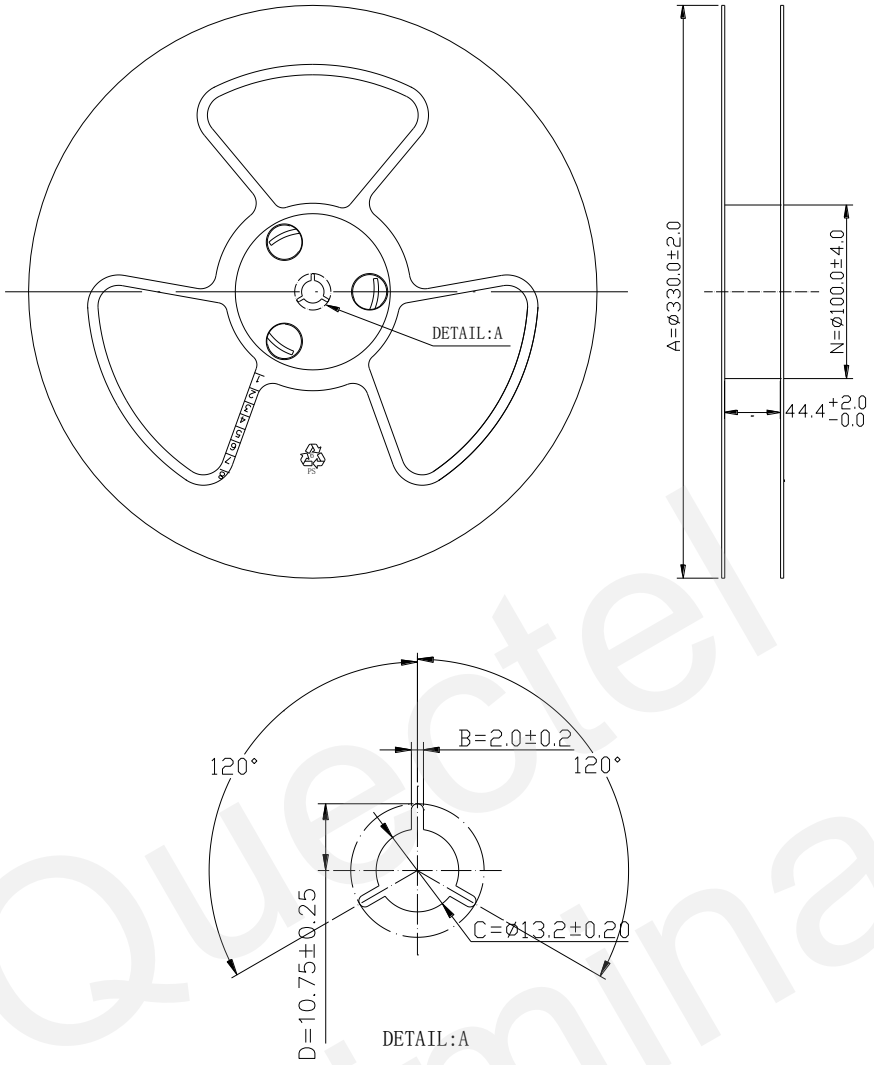

Figure 32: Reel Dimensions of UG95

Table 5: Reel Packaging Specifications of BG96/UG96/UG95

Model Name	MOQ for MP	Minimum Package: 250pcs	Minimum Package×4=1000pcs
EG9x	250pcs	Size: TBD N.W: TBD G.W: TBD	Size: TBD N.W: TBD G.W: TBD
BG96	250pcs	Size: 370mm × 350mm × 56mm N.W: TBD G.W: TBD	Size: 380mm × 250mm × 365mm N.W: TBD G.W: TBD
UG96	250pcs	Size: 370mm × 350mm × 56mm N.W: 0.78kg G.W: 1.46kg	Size: 380mm × 250mm × 365mm N.W: 3.1kg G.W: 6.45kg

UG95	250pcs	Size: 370mm × 350mm × 56mm N.W: 0.63kg G.W: 1.41kg	Size: 380mm × 250mm × 365mm N.W: 2.5kg G.W: 6.25kg

7 Appendix A References

Table 6: Related Documents

SN	Document Name	Remark
[1]	Quectel_EG91_Hardware_Design	EG91 Hardware Design
[2]	Quectel_EG95_Hardware_Design	EG95 Hardware Design
[3]	Quectel_BG96_Hardware_Design	BG96 Hardware Design
[4]	Quectel_UG96_Hardware_Design	UG96 Hardware Design
[5]	Quectel_UG95_Hardware_Design	UG95 Hardware Design
[6]	Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[7]	Quectel_EG9x_AT_Commands_Manual	AT Commands Manual for EG9x Modules
[8]	Quectel_BG96_AT_Commands_Manual	AT Commands Manual for BG96 Modules
[9]	Quectel_WCDMA_UGxx_AT_Commands_Manual	AT Commands Manual for UGxx Modules

Table 7: Terms and Abbreviations

Abbreviation	Description
DTE	Data Terminal Equipment
EDGE	Enhanced Data rates for GSM Evolution
EGPRS	Enhanced GPRS
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
GNSS	Global Navigation Satellite System

GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
HSPA	High Speed Packet Access
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
RF	Radio Frequency
SMS	Short Message Service
SWD	Serial Wire Debug
TDD	Time Division Duplexing
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module