EC21 Reference Design

LTE Module Series

Rev. EC21_Reference_Design_Rev.F

Date: 2018-02-09

Status: Released

Our aim is to provide customers with timely and comprehensive service. For any assistance, please contact our company headquarters:

Quectel Wireless Solutions Co., Ltd.
7th Floor, Hongye Building, No.1801 Hongmei Road, Xuhui District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local office. For more information, please visit:
http://quectel.com/support/sales.htm

For technical support, or to report documentation errors, please visit:
http://quectel.com/support/technical.htm
Or Email to: support@quectel.com

GENERAL NOTES

QUECTEL OFFERS THE INFORMATION AS A SERVICE TO ITS CUSTOMERS. THE INFORMATION PROVIDED IS BASED UPON CUSTOMERS' REQUIREMENTS. QUECTEL MAKES EVERY EFFORT TO ENSURE THE QUALITY OF THE INFORMATION IT MAKES AVAILABLE. QUECTEL DOES NOT MAKE ANY WARRANTY AS TO THE INFORMATION CONTAINED HEREIN, AND DOES NOT ACCEPT ANY LIABILITY FOR ANY INJURY, LOSS OR DAMAGE OF ANY KIND INCURRED BY USE OF OR RELIANCE UPON THE INFORMATION. ALL INFORMATION SUPPLIED HEREIN IS SUBJECT TO CHANGE WITHOUT PRIOR NOTICE.

COPYRIGHT

About the Document

History

Revision	Date	Author	Description
A	2016-08-22	Yeoman CHEN	Initial
B	2016-10-11	Power JIN	Added the reference design of SGMII and FC20 module
C	2016-11-11	Power JIN	1. Modified the connection of network name PCM_IN_BT and PCM_OUT_BT in Sheet 1 2. Added note 7 in Sheet 7 3. Added note 6 in Sheet 9
D	2017-01-23	Power JIN	1. Newly opened pin 37~40 for BT UART, and removed the multiplexing between Main UART and BT UART in Sheet 1 2. Modified network name TXD_MCU as RXD, RXD_MCU as TXD, CTS_MCU as CTS, RTS_MCU as RTS, RI_MCU as RI, DCD_MCU as DCD, DTR_MCU as DTR in Sheet 2 and Sheet 4 3. R904 is not mounted because SDIO_CLK in FC20 is pulled up internally 4. Modified network name PCM_IN_BT as PCM_OUT_BT, PCM_OUT_BT as PCM_IN_BT in Sheet 1 and Sheet 9 5. Modified the unidirectional off-page connectors of SDIO_CMD, SDIO_D0, SDIO_D1, SDIO_D2 and SDIO_D3 to bidirectional ones in Sheet 1 and Sheet 9
E	2017-04-01	Power JIN	1. Newly opened the SD card interface 2. Added the power supply control pin of SD card interface in Sheet 2 3. Modified the power supply circuit for PCM Codec

|			
			in Sheet 3
			4. Removed resistors R912, R913 and added resistor R0920 in Sheet 9
			5. Added the reference design for SD card interface in Sheet 10
			6. Modified the drive circuit of indicator STATUS in Sheet 11
F	2018-02-09	Woody WU	1. Changed R0110 and R0112 to L0101 on the USB differential signals in Sheet 1
			2. Added C0201, C0202 and C0203 capacitors on the PWRKEY, WAKEUP_IN_EC21 and W_DISABLE_EC21 signals in Sheet 2
			3. Deleted C0201 capacitor between Q0205 source and gate electrodes in Sheet 2
			4. Changed R0407~R0409 resistors value from 22R to 0R in Sheet 4
			5. Added R0519 and R0520 0R resistors on 17 and 20 pins of ALC5616 in Sheet 5
			6. Added TLV320AIC3104 reference design in Sheet 6
			7. Added pull-down resistors R1119~R1121 on COEX_UART_RX, COEX_UART_TX and RTS_BT signals in Sheet 11
			8. Changed STATUS reference design in Sheet 13
			9. Changed R1306 resistance from 10K to 4.7K in Sheet 13

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EC21 module.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.
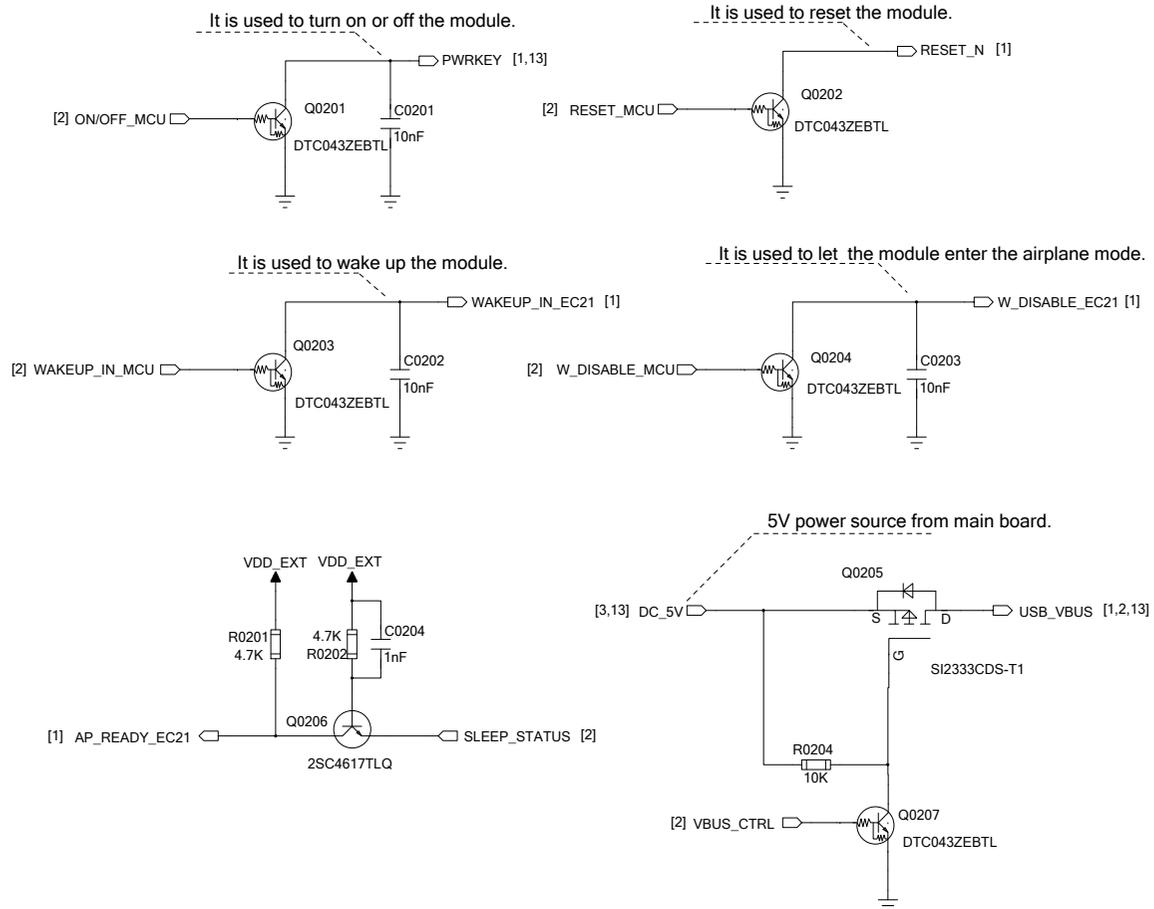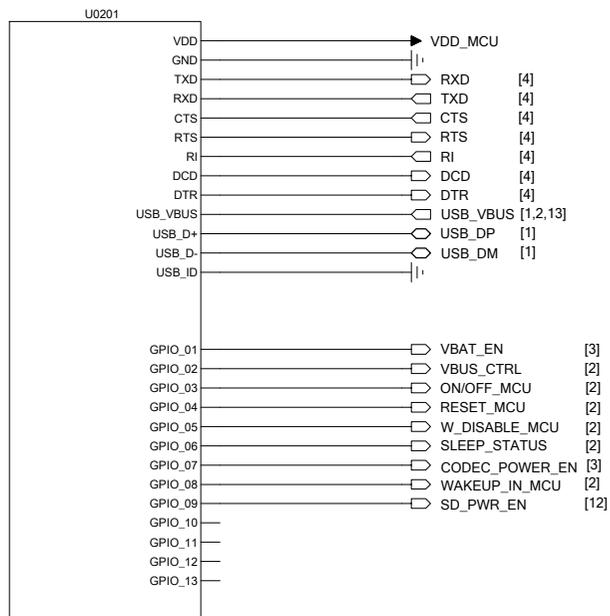
Module Interface
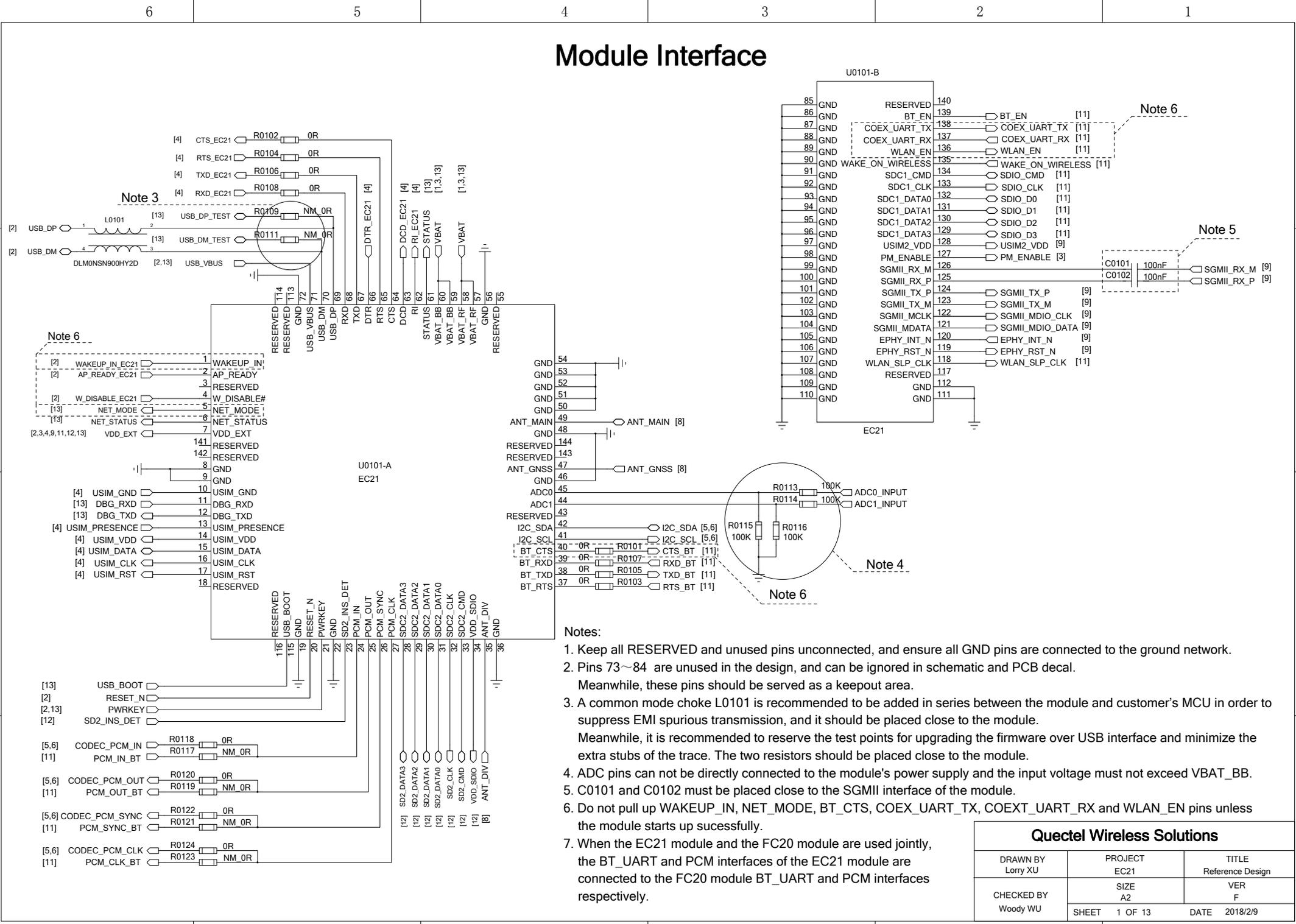
Notes:

1. Keep all RESERVED and unused pins unconnected, and ensure all GND pins are connected to the ground network.
2. Pins 73～84 are unused in the design, and can be ignored in schematic and PCB decal.
   Meanwhile, these pins should be served as a keepout area.
3. A common mode choke L0101 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission, and it should be placed close to the module.
   Meanwhile, it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace. The two resistors should be placed close to the module.
4. ADC pins can not be directly connected to the module's power supply and the input voltage must not exceed VBAT_BB.
5. C0101 and C0102 must be placed close to the SGMII interface of the module.
6. Do not pull up WAKEUP_IN, NET_MODE, BT_CTS, COEX_UART_TX, COEXT_UART_RX and WLAN_EN pins unless the module starts up sucessfully.
7. When the EC21 module and the FC20 module are used jointly, the BT_UART and PCM interfaces of the EC21 module are connected to the FC20 module BT_UART and PCM interfaces respectively.

U0101-B — EC21

Pin	Signal		Pin	Signal
85	GND	RESERVED	140	
86	GND	BT_EN	139	BT_EN [11]
87	GND	COEX_UART_TX	138	COEX_UART_TX [11]
88	GND	COEX_UART_RX	137	COEX_UART_RX [11]
89	GND	WLAN_EN	136	WLAN_EN [11]
90	GND	WAKE_ON_WIRELESS	135	WAKE_ON_WIRELESS [11]
91	GND	SDC1_CMD	134	SDIO_CMD [11]
92	GND	SDC1_CLK	133	SDIO_CLK [11]
93	GND	SDC1_DATA0	132	SDIO_D0 [11]
94	GND	SDC1_DATA1	131	SDIO_D1 [11]
95	GND	SDC1_DATA2	130	SDIO_D2 [11]
96	GND	SDC1_DATA3	129	SDIO_D3 [11]
97	GND	USIM2_VDD	128	USIM2_VDD [9]
98	GND	PM_ENABLE	127	PM_ENABLE [3]
99	GND	SGMII_RX_M	126	
100	GND	SGMII_RX_P	125	
101	GND	SGMII_TX_P	124	SGMII_TX_P [9]
102	GND	SGMII_TX_M	123	SGMII_TX_M [9]
103	GND	SGMII_MCLK	122	SGMII_MDIO_CLK [9]
104	GND	SGMII_MDATA	121	SGMII_MDIO_DATA [9]
105	GND	EPHY_INT_N	120	EPHY_INT_N [9]
106	GND	EPHY_RST_N	119	EPHY_RST_N [9]
107	GND	WLAN_SLP_CLK	118	WLAN_SLP_CLK [11]
108	GND	RESERVED	117	
109	GND	GND	112	
110	GND	GND	111	

C0101 100nF — SGMII_RX_M [9]
C0102 100nF — SGMII_RX_P [9]

Note 5
Note 6

U0101-A — EC21

[4] CTS_EC21 — R0102 0R
[4] RTS_EC21 — R0104 0R
[4] TXD_EC21 — R0106 0R
[4] RXD_EC21 — R0108 0R

Note 3

[13] USB_DP_TEST — R0109 NM_0R
[13] USB_DM_TEST — R0111 NM_0R

[2] USB_DP — L0101 — [2] USB_DM
DLM0NSN900HY2D
[2,13] USB_VBUS

Left side pins:
1	WAKEUP_IN	[2] WAKEUP_IN_EC21
2	AP_READY	[2] AP_READY_EC21
3	RESERVED	
4	W_DISABLE#	[2] W_DISABLE_EC21
5	NET_MODE	[13] NET_MODE
6	NET_STATUS	[13] NET_STATUS
7	VDD_EXT	[2,3,4,9,11,12,13] VDD_EXT
141	RESERVED	
142	RESERVED	
8	GND	
9	GND	
10	USIM_GND	[4] USIM_GND
11	DBG_RXD	[13] DBG_RXD
12	DBG_TXD	[13] DBG_TXD
13	USIM_PRESENCE	[4] USIM_PRESENCE
14	USIM_VDD	[4] USIM_VDD
15	USIM_DATA	[4] USIM_DATA
16	USIM_CLK	[4] USIM_CLK
17	USIM_RST	[4] USIM_RST
18	RESERVED	

Right side / middle:
54	GND
53	GND
52	GND
51	GND
50	GND
49	ANT_MAIN → ANT_MAIN [8]
48	GND
144	RESERVED
143	RESERVED
47	ANT_GNSS → ANT_GNSS [8]
46	GND
45	ADC0
44	ADC1
43	RESERVED
42	I2C_SDA → I2C_SDA [5,6]
41	I2C_SCL → I2C_SCL [5,6]
40	BT_CTS — 0R R0101 → CTS_BT [11]
39	BT_RXD — 0R R0107 → RXD_BT [11]
38	BT_TXD — 0R R0105 → TXD_BT [11]
37	BT_RTS — 0R R0103 → RTS_BT [11]

Note 4 / Note 6:
R0113 100K — ADC0_INPUT
R0114 100K — ADC1_INPUT
R0115 100K
R0116 100K

Bottom pins:
116	RESERVED
115	USB_BOOT — [13] USB_BOOT
19	GND
20	RESET_N — [2] RESET_N
21	PWRKEY — [2,13] PWRKEY
22	GND
23	SD2_INS_DET — [12] SD2_INS_DET
24	PCM_IN
25	PCM_OUT
26	PCM_SYNC
27	PCM_CLK
28	SDC2_DATA3 — SD2_DATA3 [12]
29	SDC2_DATA2 — SD2_DATA2 [12]
30	SDC2_DATA1 — SD2_DATA1 [12]
31	SDC2_DATA0 — SD2_DATA0 [12]
32	SDC2_CLK — SD2_CLK [12]
33	SDC2_CMD — SD2_CMD [12]
34	VDD_SDIO — VDD_SDIO [12]
35	ANT_DIV — ANT_DIV [8]
36	GND

Top pins:
114	RESERVED
113	RESERVED
72	GND
71	USB_VBUS
70	USB_DM
69	USB_DP
68	RXD
67	TXD
66	DTR — DTR_EC21 [4]
65	RTS
64	CTS
63	DCD — DCD_EC21 [4]
62	RI — RI_EC21 [4]
61	STATUS — STATUS [13][1,3,13]
60	VBAT_BB
59	VBAT_BB
58	VBAT_RF — VBAT [1,3,13]
57	VBAT_RF
56	GND
55	RESERVED

PCM / CODEC signals:
[5,6] CODEC_PCM_IN — R0118 0R / R0117 NM_0R — PCM_IN_BT [11]
[5,6] CODEC_PCM_OUT — R0120 0R / R0119 NM_0R — PCM_OUT_BT [11]
[5,6] CODEC_PCM_SYNC — R0122 0R / R0121 NM_0R — PCM_SYNC_BT [11]
[5,6] CODEC_PCM_CLK — R0124 0R / R0123 NM_0R — PCM_CLK_BT [11]

MCU Interface

U0201

Pin	Signal	Ref
VDD	VDD_MCU	
GND		
TXD	RXD	[4]
RXD	TXD	[4]
CTS	CTS	[4]
RTS	RTS	[4]
RI	RI	[4]
DCD	DCD	[4]
DTR	DTR	[4]
USB_VBUS	USB_VBUS	[1,2,13]
USB_D+	USB_DP	[1]
USB_D-	USB_DM	[1]
USB_ID		
GPIO_01	VBAT_EN	[3]
GPIO_02	VBUS_CTRL	[2]
GPIO_03	ON/OFF_MCU	[2]
GPIO_04	RESET_MCU	[2]
GPIO_05	W_DISABLE_MCU	[2]
GPIO_06	SLEEP_STATUS	[2]
GPIO_07	CODEC_POWER_EN	[3]
GPIO_08	WAKEUP_IN_MCU	[2]
GPIO_09	SD_PWR_EN	[12]
GPIO_10		
GPIO_11		
GPIO_12		
GPIO_13		

It is used to turn on or off the module.
[2] ON/OFF_MCU   Q0201   C0201   PWRKEY [1,13]
DTC043ZEBTL   10nF

It is used to reset the module.
[2] RESET_MCU   Q0202   RESET_N [1]
DTC043ZEBTL

It is used to wake up the module.
[2] WAKEUP_IN_MCU   Q0203   C0202   WAKEUP_IN_EC21 [1]
DTC043ZEBTL   10nF

It is used to let the module enter the airplane mode.
[2] W_DISABLE_MCU   Q0204   C0203   W_DISABLE_EC21 [1]
DTC043ZEBTL   10nF

VDD_EXT VDD_EXT
R0201 4.7K   4.7K R0202   C0204 1nF
[1] AP_READY_EC21   Q0206   SLEEP_STATUS [2]
2SC4617TLQ

5V power source from main board.
Q0205
[3,13] DC_5V   S   D   USB_VBUS [1,2,13]
G
SI2333CDS-T1
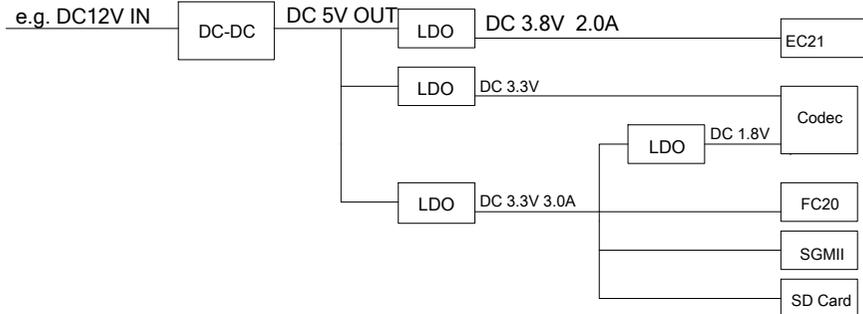R0204 10K
[2] VBUS_CTRL   Q0207
DTC043ZEBTL

Notes:
1. U0201 represents customer's MCU. The power domain of GPIO interfaces on EC21 modules is 1.8V, if the domain on U0201's GPIO interfaces is the same, then the level translation circuit can be omitted.
2. EC21 can only work as a USB device and supports Full Speed and High Speed modes. To communicate with USB interface, MCU needs to support USB host or
   OTG function. The USB_VBUS pins of MCU and EC21 should be powered by a 5V power system for USB detection, and VBUS_CTRL is used to turn on/off
   USB_VBUS power supply.
3. AP_READY is used to detect the MCU's sleep state. For more details, please refer to *Quectel_EC21_Hardware_Design*.
4. WAKEUP_IN_EC21 should should be kept at low level before the module starts up successfully.
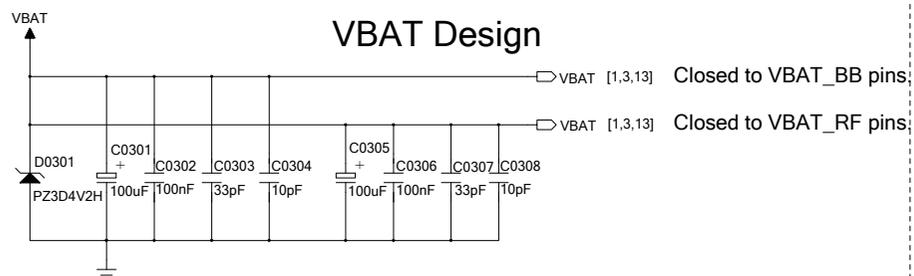
Power Supply Design

DC-DC Application

It is used when the input voltage is above 7V. Use a DC-DC converter to convert a high input voltage into a 5V output, and then the LDOs will generate 3.8V, 3.3V and 1.8V typical voltages.

e.g. DC12V IN → DC-DC → DC 5V OUT → LDO → DC 3.8V 2.0A → EC21

LDO → DC 3.3V → Codec

LDO → DC 1.8V → Codec

LDO → DC 3.3V 3.0A → FC20 / SGMII / SD Card

VBAT Design

VBAT [1,3,13] Closed to VBAT_BB pins
VBAT [1,3,13] Closed to VBAT_RF pins

D0301 PZ3D4V2H

C0301 100uF C0302 100nF C0303 33pF C0304 10pF C0305 100uF C0306 100nF C0307 33pF C0308 10pF
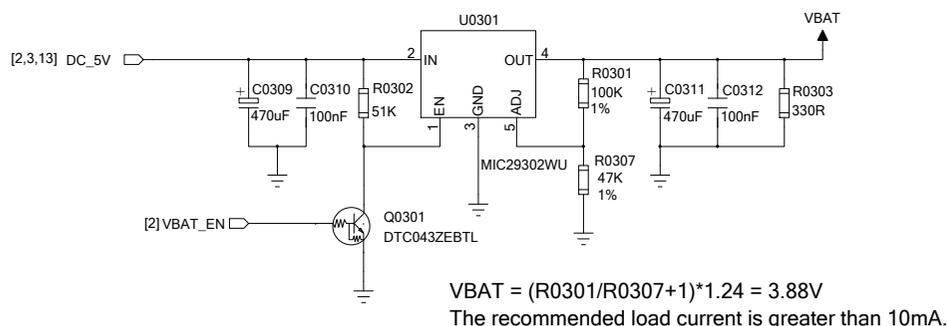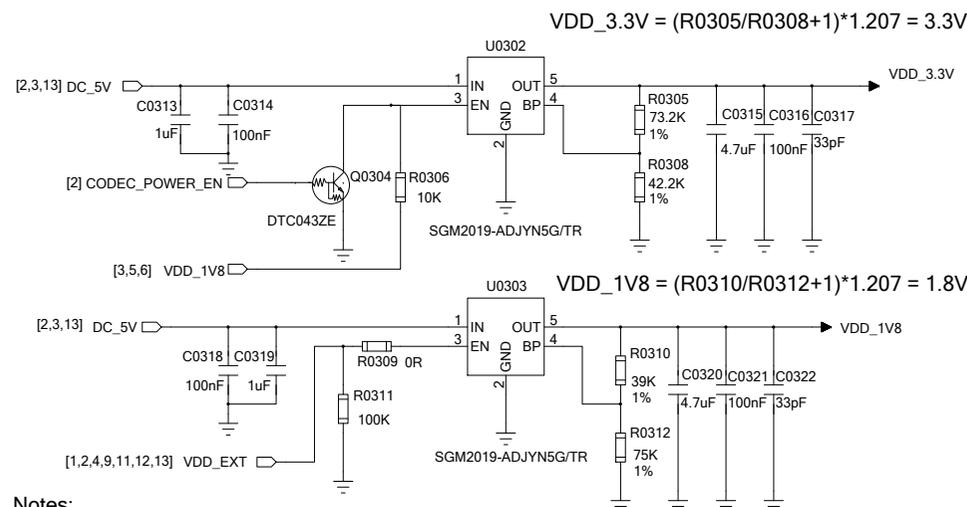
Notes:
1. The power supply must be able to provide sufficient current up to 2A or more.
2. VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.3V～4.3V.

LDO Application
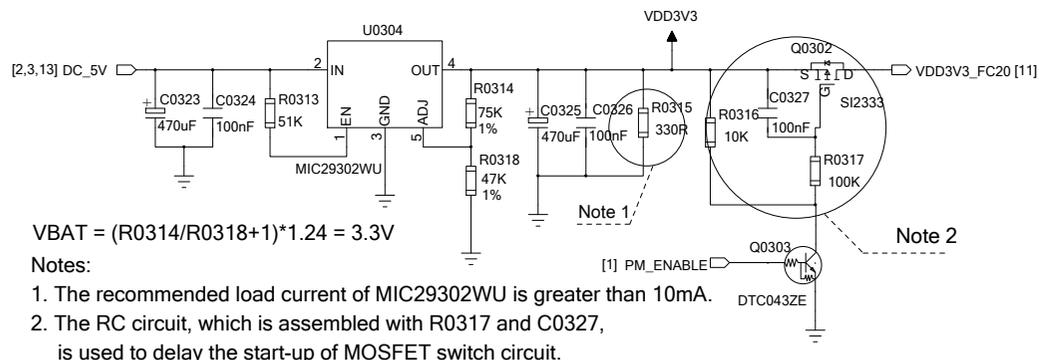
It is used when the input voltage is below 7V.

U0301 MIC29302WU

[2,3,13] DC_5V

C0309 470uF C0310 100nF R0302 51K

IN OUT ADJ EN GND

R0301 100K 1% C0311 470uF C0312 100nF R0303 330R

R0307 47K 1%

VBAT

[2] VBAT_EN Q0301 DTC043ZEBTL

$VBAT = (R0301/R0307+1)*1.24 = 3.88V$
The recommended load current is greater than 10mA.

Power Supply for PCM Codec

$VDD\_3.3V = (R0305/R0308+1)*1.207 = 3.3V$

U0302 SGM2019-ADJYN5G/TR

[2,3,13] DC_5V

C0313 1uF C0314 100nF

IN EN OUT BP GND

[2] CODEC_POWER_EN Q0304 DTC043ZE R0306 10K

[3,5,6] VDD_1V8

R0305 73.2K 1% C0315 4.7uF C0316 100nF C0317 33pF

R0308 42.2K 1%

VDD_3.3V

$VDD\_1V8 = (R0310/R0312+1)*1.207 = 1.8V$

U0303 SGM2019-ADJYN5G/TR

[2,3,13] DC_5V

C0318 100nF C0319 1uF

R0309 0R

IN EN OUT BP GND

R0311 100K

[1,2,4,9,11,12,13] VDD_EXT

R0310 39K 1% C0320 4.7uF C0321 100nF C0322 33pF

R0312 75K 1%

VDD_1V8

Notes:
1. CODEC_POWER_EN must be at low level in order to ensure the normal output voltage of VDD_3.3V. If VDD_3.3V power supply needs to be switched off, please keep CODEC_POWER_EN at high level.
2. The following power-on/off sequences should be complied with to ensure the audio codec works normally.
   Power-on Sequence: power on VDD_1V8 first, then VDD_3.3V.
   Power-off Sequence: power off VDD_3.3V first, then VDD_1V8.
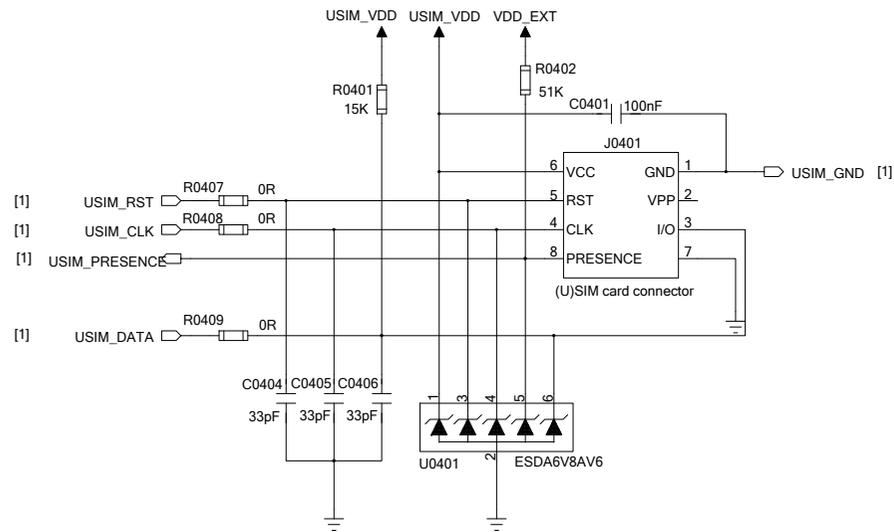
Power Supply for FC20, SGMII and SD Card

U0304 MIC29302WU

[2,3,13] DC_5V

C0323 470uF C0324 100nF R0313 51K

IN OUT ADJ EN GND

R0314 75K 1% C0325 470uF C0326 100nF R0315 330R

R0318 47K 1%

Note 1

VDD3V3

Q0302 SI2333 S G D C0327 100nF R0316 10K R0317 100K

VDD3V3_FC20 [11]

Note 2

[1] PM_ENABLE Q0303 DTC043ZE

$VBAT = (R0314/R0318+1)*1.24 = 3.3V$

Notes:
1. The recommended load current of MIC29302WU is greater than 10mA.
2. The RC circuit, which is assembled with R0317 and C0327, is used to delay the start-up of MOSFET switch circuit.

(U)SIM and UART Designs

(U)SIM Interface

USIM_VDD USIM_VDD VDD_EXT

R0401 15K
R0402 51K
C0401 100nF

J0401

6 VCC   GND 1   USIM_GND [1]
5 RST   VPP 2
4 CLK   I/O 3
8 PRESENCE   7

(U)SIM card connector

[1] USIM_RST   R0407 0R
[1] USIM_CLK   R0408 0R
[1] USIM_PRESENCE

[1] USIM_DATA   R0409 0R

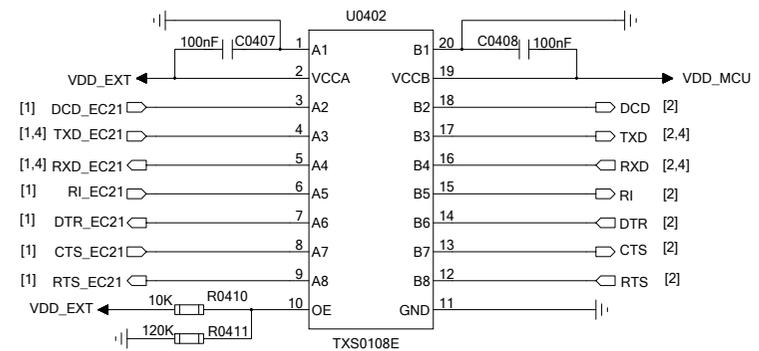C0404 33pF   C0405 33pF   C0406 33pF

U0401   ESDA6V8AV6

Notes:
1. U401 is recommended to be used to offer good ESD protection,
   and the parasitic capacitance should not be more than 15pF.
2. It is recommended to connect the (U)SIM card connector GND to the module USIM_GND.
   If the ground is complete on customers' PCB, USIM_GND can be connected to PCB ground directly.
3. The pull-up resistor R0401 can improve anti-jamming capability,
   and should be placed close to the (U)SIM card connector.
4. R0407～R0409 are used for debugging,
   C0404～C0406 are used for filtering interference of GSM900MHz.
5. C0401 capacitance should be less than 1uF,
   and should be placed close to the (U)SIM card connector.
6. For more information about the layout, please refer to *Quectel_EC21_Hardware_Design*.

UART Translation - Transistor Solution

VDD_EXT VDD_EXT

C0403 1nF   R0405 10K   R0406 10K

[2,4] RXD   Q0401   RXD_EC21 [1,4]
2SC4617TLQ

VDD_MCU VDD_EXT

R0403 10K   R0404 10K   C0402 1nF

[2,4] TXD   Q0402   TXD_EC21 [1,4]
2SC4617TLQ
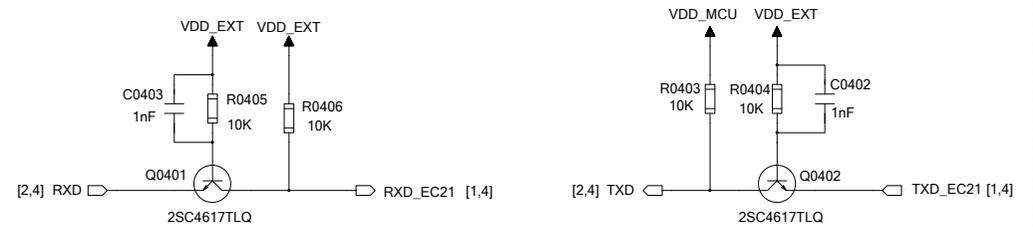
UART Translation - IC Solution

U0402

100nF C0407

1 A1   B1 20   C0408 100nF
2 VCCA   VCCB 19   VDD_MCU
VDD_EXT
3 A2   B2 18   DCD [2]
[1] DCD_EC21
4 A3   B3 17   TXD [2,4]
[1,4] TXD_EC21
5 A4   B4 16   RXD [2,4]
[1,4] RXD_EC21
6 A5   B5 15   RI [2]
[1] RI_EC21
7 A6   B6 14   DTR [2]
[1] DTR_EC21
8 A7   B7 13   CTS [2]
[1] CTS_EC21
9 A8   B8 12   RTS [2]
[1] RTS_EC21
10 OE   GND 11
VDD_EXT   10K   R0410
120K   R0411

TXS0108E

Notes:
1. There are two translation solutions: transistor solution and IC solution,
   and it is recommended to select the IC solution.
2. The power supply voltage of VCCA should not exceed that of VCCB.
   For more information about TXS0108E, please refer to the datasheet from TI.
3. The transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.
   The 1nF capacitors C0402 and C0403 can improve the signal quality.
4. The RTS and DTR transistor circuits are similar to that of RXD interface.
   The CTS, RI and DCD transistor circuits are similar to that of TXD interface.

Quectel Wireless Solutions

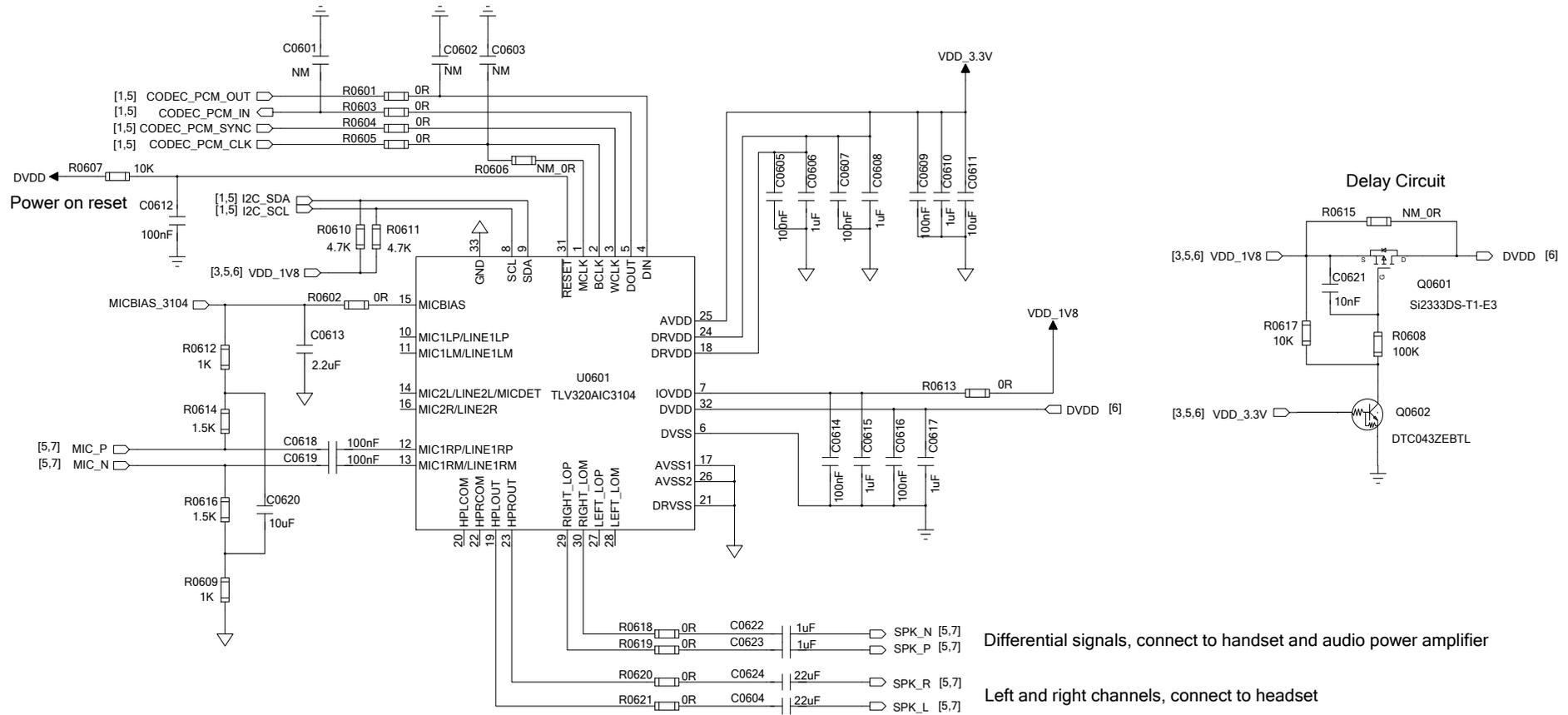| DRAWN BY Lorry XU | PROJECT EC21 | TITLE Reference Design |
| CHECKED BY Woody WU | SIZE A2 | VER F |
| | SHEET 4 OF 13 | DATE 2018/2/9 |

Audio Codec Design (ALC5616)
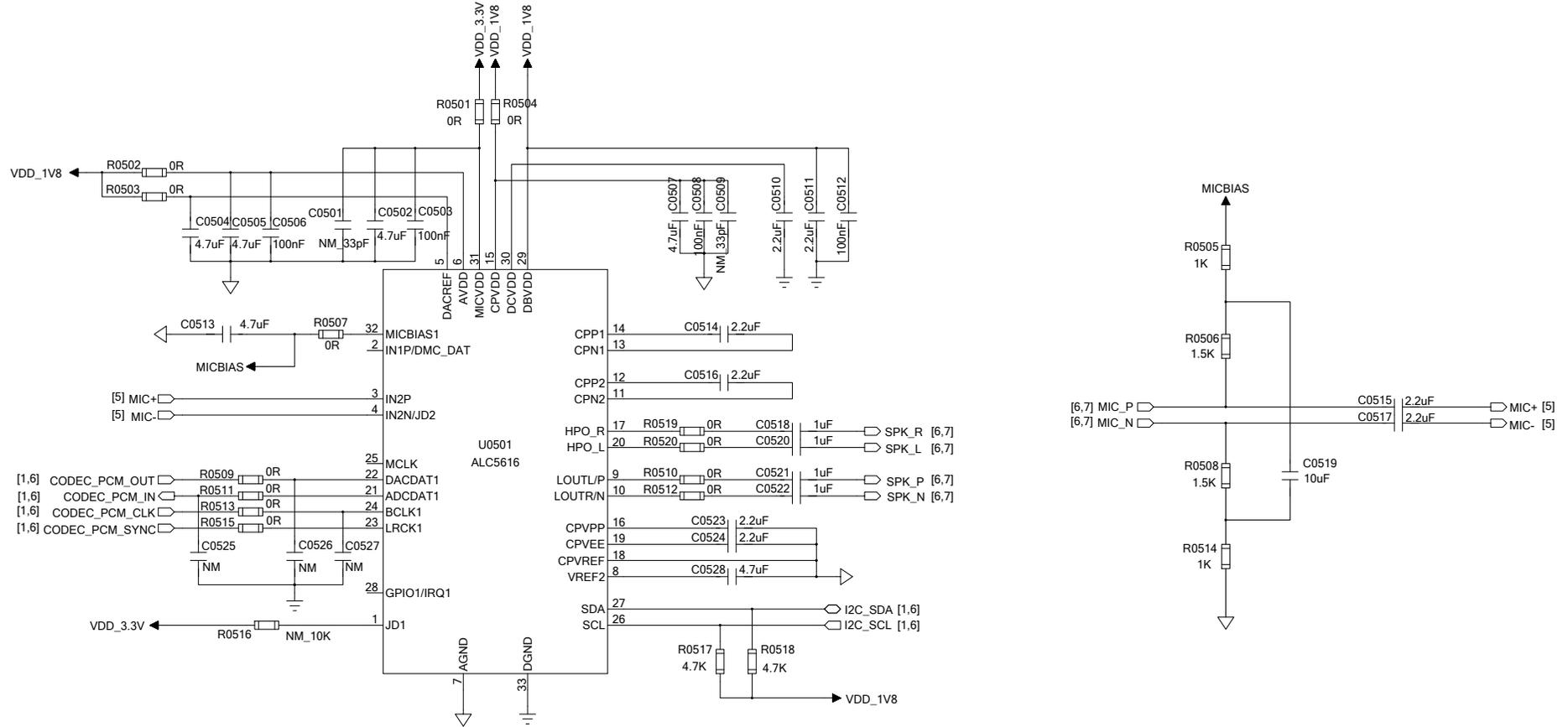
Notes:
1. ALC5616 power-on sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD -> MICVDD -> software initialization.
2. ALC5616 power-off sequence: close codec function by software-> MICVDD -> DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. EC21 module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be powered on before that.

Audio Codec Design (TLV320AIC3104)

Delay Circuit

Power on reset

MICBIAS_3104

U0601
TLV320AIC3104

[1,5] CODEC_PCM_OUT
[1,5] CODEC_PCM_IN
[1,5] CODEC_PCM_SYNC
[1,5] CODEC_PCM_CLK

R0601 0R
R0603 0R
R0604 0R
R0605 0R

C0601 NM
C0602 NM
C0603 NM

R0607 10K
DVDD

C0612 100nF

[1,5] I2C_SDA
[1,5] I2C_SCL

R0610 4.7K
R0611 4.7K

[3,5,6] VDD_1V8

R0602 0R

R0606 NM_0R

VDD_3.3V

C0605 100nF
C0606 1uF
C0607 100nF
C0608 1uF
C0609 100nF
C0610 1uF
C0611 10uF

R0612 1K

C0613 2.2uF

R0614 1.5K

[5,7] MIC_P
[5,7] MIC_N

C0618 100nF
C0619 100nF

R0616 1.5K
C0620 10uF

R0609 1K

15 MICBIAS
10 MIC1LP/LINE1LP
11 MIC1LM/LINE1LM
14 MIC2L/LINE2L/MICDET
16 MIC2R/LINE2R
12 MIC1RP/LINE1RP
13 MIC1RM/LINE1RM

33 GND
8 SCL
9 SDA
31 RESET
1 MCLK
2 BCLK
3 WCLK
5 DOUT
4 DIN

25 AVDD
24 DRVDD
18 DRVDD
7 IOVDD
32 DVDD
6 DVSS
17 AVSS1
26 AVSS2
21 DRVSS

20 HPLCOM
22 HPRCOM
19 HPLOUT
23 HPROUT
29 RIGHT_LOP
30 RIGHT_LOM
27 LEFT_LOP
28 LEFT_LOM

VDD_1V8

R0613 0R
DVDD [6]

C0614 100nF
C0615 1uF
C0616 100nF
C0617 1uF

R0615 NM_0R
[3,5,6] VDD_1V8
DVDD [6]
C0621 10nF
Q0601 Si2333DS-T1-E3
R0617 10K
R0608 100K

[3,5,6] VDD_3.3V
Q0602 DTC043ZEBTL

R0618 0R C0622 1uF SPK_N [5,7]
R0619 0R C0623 1uF SPK_P [5,7]
R0620 0R C0624 22uF SPK_R [5,7]
R0621 0R C0604 22uF SPK_L [5,7]

Differential signals, connect to handset and audio power amplifier

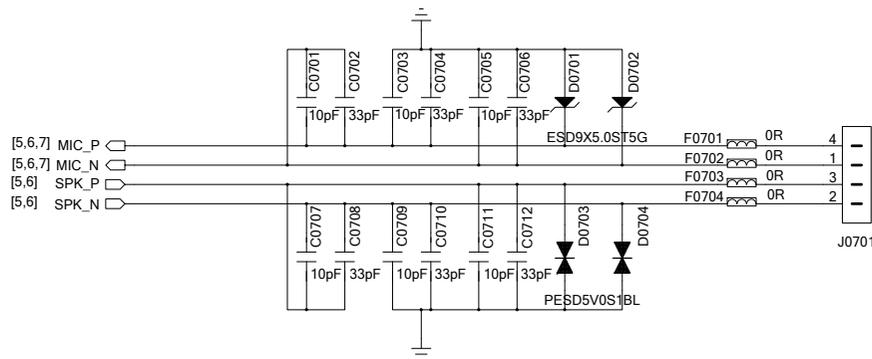Left and right channels, connect to headset

Notes:
1. TLV320AIC3104 power-on sequence: IOVDD -> AVDD/DRVDD -> DVDD -> software initialization.
2. The RC delay circuit, which is assembled with C0621 and R0608, is used to ensure that the power-on time difference between AVDD and DVDD is within 5ms.
3. The RESET pin must be driven at low level for at least 10ns after all power supplies for TLV320AIC3104 are at their specified values.
4. EC21 module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be powered on before that.

Audio Interface

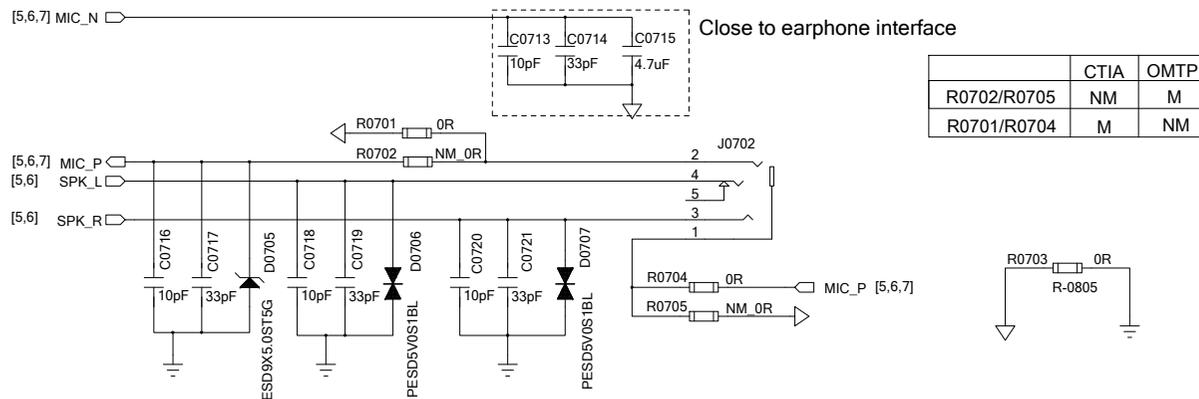## Handset Application

[5,6,7] MIC_P
[5,6,7] MIC_N
[5,6] SPK_P
[5,6] SPK_N

C0701 10pF C0702 33pF C0703 10pF C0704 33pF C0705 10pF C0706 33pF D0701 D0702
ESD9X5.0ST5G

C0707 10pF C0708 33pF C0709 10pF C0710 33pF C0711 10pF C0712 33pF D0703 D0704
PESD5V0S1BL

F0701 0R   4
F0702 0R   1
F0703 0R   3
F0704 0R   2
J0701

Earphone Application

[5,6,7] MIC_N

Close to earphone interface

C0713 10pF C0714 33pF C0715 4.7uF

R0701 0R
R0702 NM_0R

[5,6,7] MIC_P
[5,6] SPK_L
[5,6] SPK_R

J0702
2
4
5
3
1

C0716 10pF C0717 33pF D0705 ESD9X5.0ST5G C0718 10pF C0719 33pF D0706 PESD5V0S1BL C0720 10pF C0721 33pF D0707 PESD5V0S1BL

R0704 0R   MIC_P [5,6,7]
R0705 NM_0R

R0703 0R
R-0805

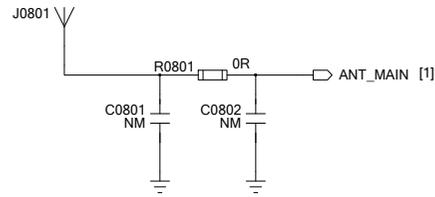|	CTIA	OMTP
R0702/R0705	NM	M
R0701/R0704	M	NM

Notes:

1. The analog output only drives earphone and headset. For larger power loads such as speakers, an audio power amplifier should be added in the design.

2. In handset application, both the MIC and SPK signal traces need to be routed as differential pairs.

3. In earphone application, the MIC signal traces need to be routed as differential pairs.

4. All MIC and SPK signal traces should be routed with total grounding and far away from noise such as clock and DC-DC signals, etc.

5. ALC5616 and TLV320AIC3104 cannot be used simultaneously in audio codec design.
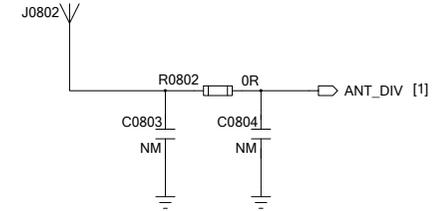
Quectel Wireless Solutions

DRAWN BY Lorry XU	PROJECT EC21	TITLE Reference Design
CHECKED BY Woody WU	SIZE A2	VER F
	SHEET 7 OF 13	DATE 2018/2/9

RF and GNSS Designs

Main Antenna Circuit

J0801

R0801 0R ▷ ANT_MAIN [1]

C0801 NM C0802 NM

Diversity Antenna Circuit

J0802

R0802 0R ▷ ANT_DIV [1]

C0803 NM C0804 NM

GNSS Antenna Circuit

VDD

C0805 0.1uF R0803 10R

J0804

L0801 47nH

Active Antenna
Passive Antenna

C0808 100pF ▷ ANT_GNSS [1]

C0809 NM C0810 NM

FC20 Antenna Circuit

J0803

R0804 0R ▷ FC20_ANT [11]

C0806 NM C0807 NM
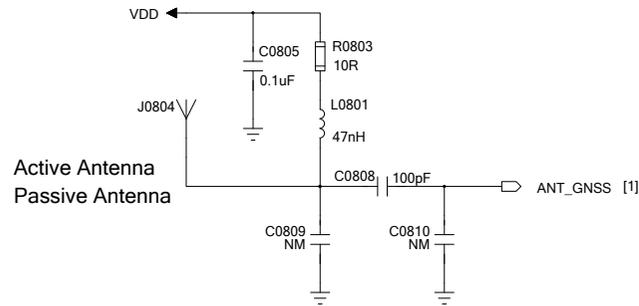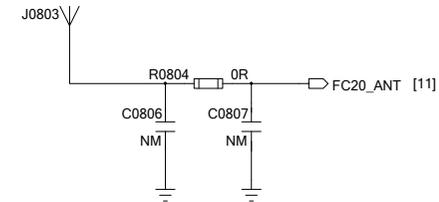
Notes:
1. It is recommended to use PI type main/Rx-diversity/FC20 antenna circuit, thus ensuring convenient subsequent debugging.
2. The diversity reception function is ON by default. If diversity antenna is not used, there is a need to use AT command to turn off diversity reception.
3. An external LDO can be selected to supply power for active antenna.
4. If passive antenna is used, then R0803 and L0801 are not needed.
5. The impedance of the RF signal traces must be controlled as 50Ω when routing.

Quectel Wireless Solutions		
DRAWN BY Lorry XU	PROJECT EC21	TITLE Reference Design
CHECKED BY	SIZE A2	VER F
Woody WU	SHEET 8 OF 13	DATE 2018/2/9

Ethernet PHY Design

SGMII_MDIO_DAT should be connected to the USIM2_VDD beside the module with a 1.5K pull-up resistor.

To minimize crosstalk, the reset trace must be at least 20 mils away from other signal traces.

[1] SGMII_MDIO_DATA
[1] SGMII_MDIO_CLK
[1] EPHY_RST_N

R904   0R

C910   NM_1uF

L0901, C0913 and C0914 need to be placed close to Pin 3.

[9] DVDD_1V1
[9] VDD33_SGMII

L901
4.7uH

C911   C912   C913   C914
10uF   0.1uF   10uF   0.1uF

VDD_EXT   R908   10K
[1] EPHY_INT_N

[1,2,3,4,11,12,13]

Y901

2 GND XTAL 3
4 GND XTAL 1

25MHz

C917   C918
10pF   10pF

[9] AVDD_1V1
[9] VDDH_2V5
[10] TRXP0
[10] TRXN0

R916
2.37K 1%

C921   C922
0.1uF   1uF

The two capacitors should be selected according to the actual load capacitance of crystal and the board-level test results.

R916 should be placed close to AR8033.
The traces of the resistor must be away from other traces (especially the clock and MDI interface traces), and the trace width needs to be at least 25 mils.

USIM2_VDD [1]
VDDH_2V5 [9]

R902   R903
1.5K   NM_100K

DVDD_1V1 [9]
FB901
BLM15AX700SN1D

AVDD_1V1 [9]

C905   C906   C907
0.1uF   2.2uF   0.1uF

Close to AR8033

C908   0.1uF
C909   0.1uF

[9] VDD33_SGMII

C901   C902   C903   C904
10pF   33pF   100nF   100uF

R901   0R   VDD3V3 [3,12]

SGMII_TX_P [1]
SGMII_TX_M [1]
SGMII_RX_P [1]
SGMII_RX_M [1]

R905   NM_10K   AVDD_1V1 [9]
R906   NM_10K   VDD33_SGMII [9]

49 48 47 46 45 44 43 42 41 40 39 38 37
GND MDIO DVDDL SIP SIN AVDDL SOP SON SD WOL_INT TXD3 TXD2 TXD1

U901
AR8033-AL1B-R

1 MDC
2 RSTN
3 LX
4 VDD33
5 INT
6 XTLO
7 XTLI
8 AVDDL
9 RBIAS
10 VDDH_REG
11 TRXP0
12 TRXN0

TXD0   36
GTX_CLK 35
TX_EN   34
RX_CLK 33   MODE 2   R909   10K
RX_DV   32   MODE 0   R910   10K
RXD0   31   PHY_AD0   R911   10K
RXD1   30   PHY_AD1   R912   10K
VDDIO_REG 29
RXD2   28   MODE 1   R913   10K
RXD3   27   MODE 3   R914   10K
LED_10_100 26
CLK_25M 25

C919   C920
NM   NM/470pF

13 14 15 16 17 18 19 20 21 22 23 24
AVDDL TRXP1 TRXN1 AVDD33 TRXP2 TRXN2 AVDDL TRXP3 TRXN3 NC LED_ACT LED_1000

AVDD_1V1   AVDD_1V1   PHY_AD2

[9] AVDD_1V1

C925
0.1uF

C926
0.1uF

[9] VDD33_SGMII   FB902
BLM15AX700SN1D

C927   C928
1uF   0.1uF

VDDH_2V5 [9]

R907   0R

C915   C916
100pF   0.1uF

D901   R915   510R

GREEN

CLK_25M

C923   NM/470pF
C924   NM/470pF

EMI filter is reserved.
If LED pins are not used, keep C0920/C0923/C0924=470pF.

R917   10K
R918   10K   EXT_INT_SEL

LED_1000 [10]
LED_ACT   [10]
TRXN3   [10]
TRXP3   [10]
TRXN2   [10]
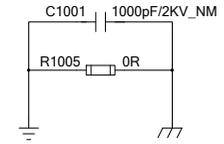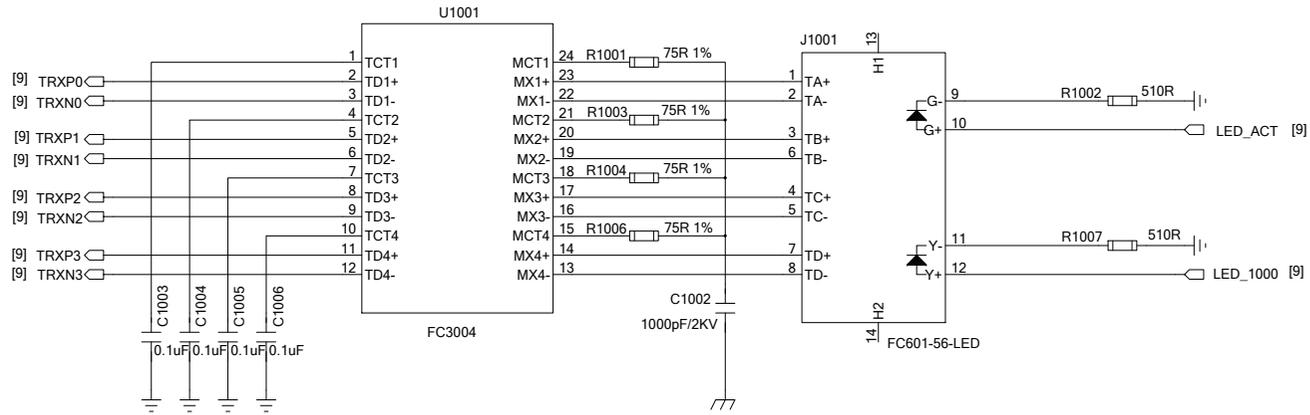TRXP2   [10]
TRXN1   [10]
TRXP1   [10]

Notes:
1. In the following description, the SGMII data signal refers to the SGMII TX and RX difference pair, and the SGMII control signal refers to the SGMII_MDIO_CLK, SGMII_MDIO_DATA, EPHY_RST_N and EPHY_INT_N.
2. SGMII data and control signals should be strictly protected with ground and kept away from RF, analog, clock and DCDC signals etc.
3. Keep the maximum trace length of SGMII data signal less than 10-inch and keep skew of the TX and RX signals less than 20mil.
4. The differential impedance of SGMII data signal is 100Ω±10%, and the reference ground of the area should be complete.
5. Make sure the trace spacing between SGMII RX and TX is at least 3 times of the trace width, and the same to the adjacent signal traces.
6. The peripheral circuit layout of Ethernet PHY chip AR8033 should be designed on a four-layer PCB,
   and the second layer should be total grounded as the AR8033 reference GND.
7. RJ45, network transformer, AR8033, and the SGMII interface should be placed close to each other.

Ethernet Network Port Design

U1001

1	TCT1	
2	TD1+	
3	TD1-	
4	TCT2	
5	TD2+	
6	TD2-	
7	TCT3	
8	TD3+	
9	TD3-	
10	TCT4	
11	TD4+	
12	TD4-	

[9] TRXP0
[9] TRXN0
[9] TRXP1
[9] TRXN1
[9] TRXP2
[9] TRXN2
[9] TRXP3
[9] TRXN3

FC3004

24	MCT1	R1001 75R 1%	1	TA+
23	MX1+		2	TA-
22	MX1-	R1003 75R 1%	
21	MCT2		3	TB+
20	MX2+		6	TB-
19	MX2-	R1004 75R 1%	
18	MCT3		4	TC+
17	MX3+		5	TC-
16	MX3-	R1006 75R 1%	
15	MCT4		7	TD+
14	MX4+		8	TD-
13	MX4-		

C1003 0.1uF
C1004 0.1uF
C1005 0.1uF
C1006 0.1uF

C1002 1000pF/2KV

J1001
13 H1
14 H2
FC601-56-LED

G- 9 R1002 510R
G+ 10 LED_ACT [9]
Y- 11 R1007 510R
Y+ 12 LED_1000 [9]

C1001 1000pF/2KV_NM
R1005 0R

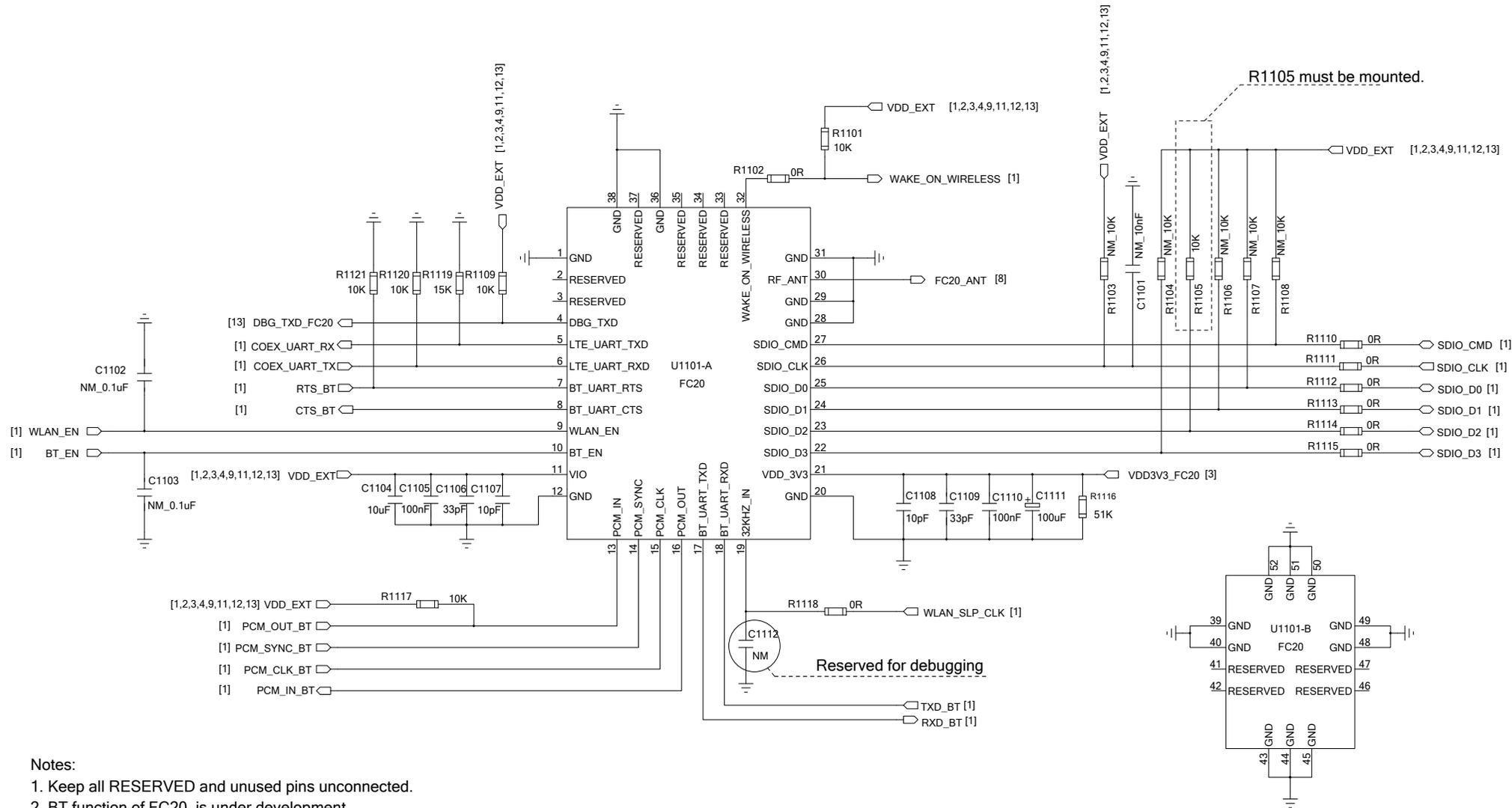| PHY core configuration signal	Description	Default internal weak pull-up/down	Application external weak pull-up/down
PHY_AD2	PHY_AD[2:0] set the lower three bits of the physical address. The upper two bits of the physical address are set to 00.	1	0
PHY_AD1		0	0
PHY_AD0		0	0
MODE 3	Mode select bit 3	0	0
MODE 2	Mode select bit 2	0	0
MODE 1	Mode select bit 1	0	0
MODE 0	Mode select bit 0	0	1
EXT_INT_SEL	An external 10K pull-down resistor is required.	1	0
0 = Pull-down, 1 = Pull-up.			

Notes:
1. Route MDI differential signals with 100Ω±10%, and the reference ground of the area should be complete.
2. Keep skew of the MDI differential signals less than 20mils, and the maximum trace length must be less than10 inches.
3. To minimize crosstalk, the distance between separate adjacent pairs that are on the same layer must be equal to or larger than 40 mils.

FC20 Design

R1105 must be mounted.

VDD_EXT [1,2,3,4,9,11,12,13]

R1101 10K

R1102 0R WAKE_ON_WIRELESS [1]

VDD_EXT [1,2,3,4,9,11,12,13]

VDD_EXT [1,2,3,4,9,11,12,13]

VDD_EXT [1,2,3,4,9,11,12,13]

R1103 NM_10K
C1101 NM_10nF
R1104 NM_10K
R1105 10K
R1106 NM_10K
R1107 NM_10K
R1108 NM_10K

U1101-A FC20

Pin	Signal
38	GND
37	RESERVED
36	GND
35	RESERVED
34	RESERVED
33	RESERVED
32	WAKE_ON_WIRELESS
1	GND
2	RESERVED
3	RESERVED
4	DBG_TXD
5	LTE_UART_TXD
6	LTE_UART_RXD
7	BT_UART_RTS
8	BT_UART_CTS
9	WLAN_EN
10	BT_EN
11	VIO
12	GND
13	PCM_IN
14	PCM_SYNC
15	PCM_CLK
16	PCM_OUT
17	BT_UART_TXD
18	BT_UART_RXD
19	32KHZ_IN

Pin	Signal
31	GND
30	RF_ANT
29	GND
28	GND
27	SDIO_CMD
26	SDIO_CLK
25	SDIO_D0
24	SDIO_D1
23	SDIO_D2
22	SDIO_D3
21	VDD_3V3
20	GND

FC20_ANT [8]

R1121 10K R1120 10K R1119 15K R1109 10K

[13] DBG_TXD_FC20
[1] COEX_UART_RX
[1] COEX_UART_TX
[1] RTS_BT
[1] CTS_BT
[1] WLAN_EN
[1] BT_EN
[1,2,3,4,9,11,12,13] VDD_EXT

C1102 NM_0.1uF
C1103 NM_0.1uF

C1104 10uF C1105 100nF C1106 33pF C1107 10pF

R1110 0R SDIO_CMD [1]
R1111 0R SDIO_CLK [1]
R1112 0R SDIO_D0 [1]
R1113 0R SDIO_D1 [1]
R1114 0R SDIO_D2 [1]
R1115 0R SDIO_D3 [1]

VDD3V3_FC20 [3]

C1108 10pF C1109 33pF C1110 100nF C1111 100uF R1116 51K

[1,2,3,4,9,11,12,13] VDD_EXT R1117 10K
[1] PCM_OUT_BT
[1] PCM_SYNC_BT
[1] PCM_CLK_BT
[1] PCM_IN_BT

R1118 0R WLAN_SLP_CLK [1]

C1112 NM

Reserved for debugging

TXD_BT [1]
RXD_BT [1]

U1101-B FC20

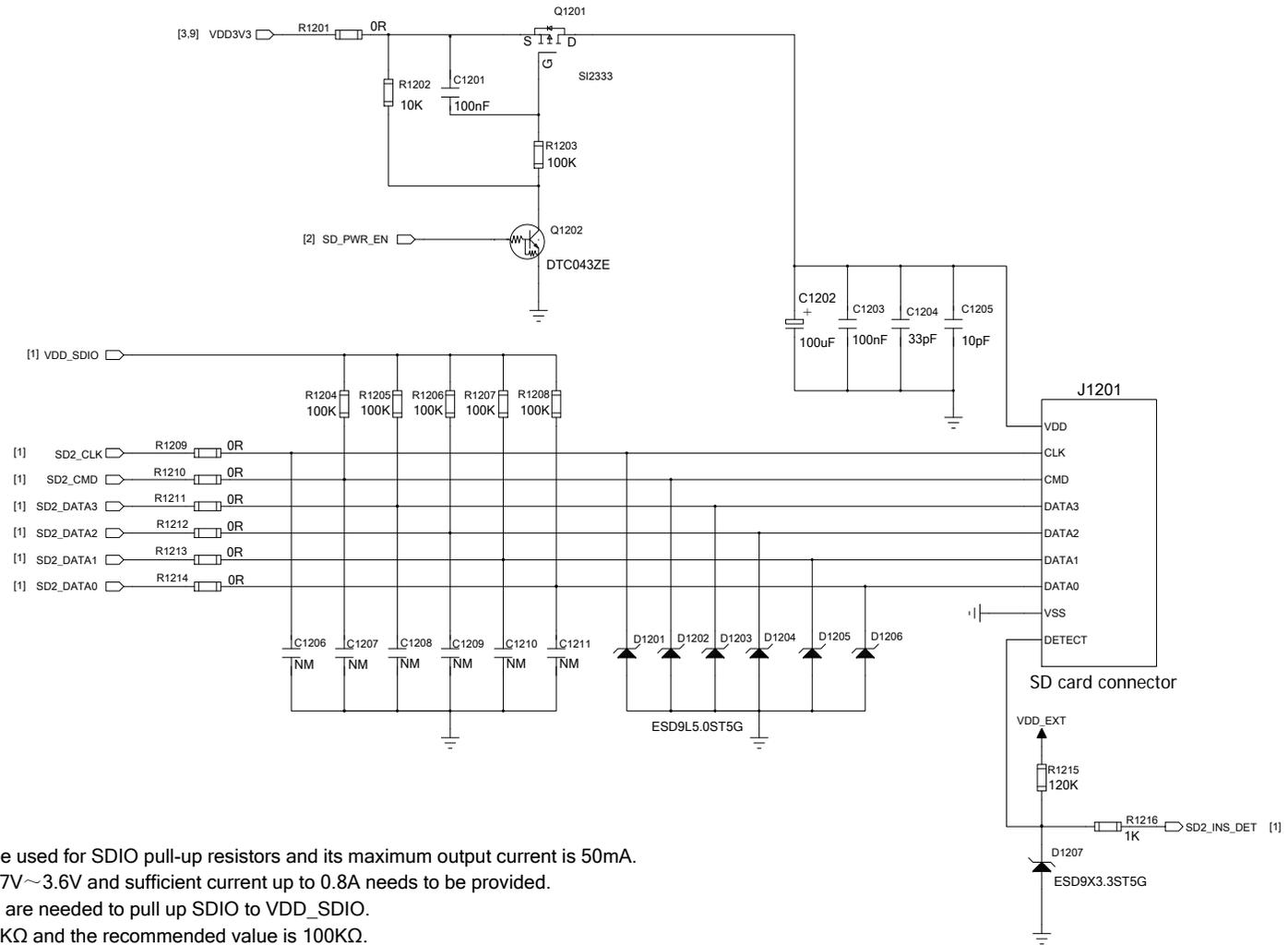| Pin	Signal
52	GND
51	GND
50	GND
39	GND
40	GND
41	RESERVED
42	RESERVED
49	GND
48	GND
47	RESERVED
46	RESERVED
43	GND
44	GND
45	GND

Notes:
1. Keep all RESERVED and unused pins unconnected.
2. BT function of FC20 is under development.
3. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock and DC-DC signals, etc.
4. Route SDIO signals with 50Ω±10% impedance. It is important to route the SDIO signal traces with total grounding, and the total routing length should be less than 50mm.
5. It is recommended to keep the matching length between CLK and DATA/CMD less than 1mm.
6. Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 15pF.
7. The pins 5～8, 10, 13～18 should be unconnected when using FC20-N.
8. FC20 power-on sequence: VIO -> VDD_3V3.

SD Card Interface Design

[3,9] VDD3V3   R1201   0R

Q1201
S   D
SI2333

R1202 10K   C1201 100nF

R1203 100K

[2] SD_PWR_EN   Q1202   DTC043ZE

C1202 + 100uF   C1203 100nF   C1204 33pF   C1205 10pF

[1] VDD_SDIO

R1204 100K   R1205 100K   R1206 100K   R1207 100K   R1208 100K

J1201
VDD
CLK
CMD
DATA3
DATA2
DATA1
DATA0
VSS
DETECT

SD card connector

[1] SD2_CLK   R1209 0R
[1] SD2_CMD   R1210 0R
[1] SD2_DATA3   R1211 0R
[1] SD2_DATA2   R1212 0R
[1] SD2_DATA1   R1213 0R
[1] SD2_DATA0   R1214 0R

C1206 NM   C1207 NM   C1208 NM   C1209 NM   C1210 NM   C1211 NM

D1201 D1202 D1203 D1204 D1205 D1206

ESD9L5.0ST5G

VDD_EXT

R1215 120K

R1216 1K   SD2_INS_DET [1]

D1207 ESD9X3.3ST5G

Notes:
1. The pin 34 (VDD_SDIO) on the module can only be used for SDIO pull-up resistors and its maximum output current is 50mA.
2. The supply voltage range of VDD for SD card is 2.7V～3.6V and sufficient current up to 0.8A needs to be provided.
3. To avoid the jitter of bus, resistors R1204～R1208 are needed to pull up SDIO to VDD_SDIO.
   The value of these resistors is among 10KΩ～100KΩ and the recommended value is 100KΩ.
4. In order to adjust signal quality, it is recommended to add 0Ω resistors R1209～R1214 in series between the module and the SD card connector.
   The bypass capacitors C1206～C1211 are reserved and not mounted by default.
5. It is recommended to add ESD protection devices near the pins of SD card connector. The parasitic capacitance of ESD protection devices should be smaller than 15pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock and DC-DC signals, etc.
7. Route SDIO signals with 50Ω±10% impedance. It is important to route SDIO signals with total grounding, and the total trace length should be less than 23mm.
8. It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm.
9. Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 15pF.

Quectel Wireless Solutions

DRAWN BY Lorry XU	PROJECT EC21	TITLE Reference Design
CHECKED BY Woody WU	SIZE A2	VER F
	SHEET 12OF 13	DATE 2018/2/9

Other Designs

Indicators

VBAT

D1312

R1307
2.2K

[1] STATUS

DC_5V

D1301

R1303
2.2K

[1] NET_MODE

Q1302
DTC043ZEBTL

DC_5V

D1302

R1304
2.2K

[1] NET_STATUS

Q1303
DTC043ZEBTL
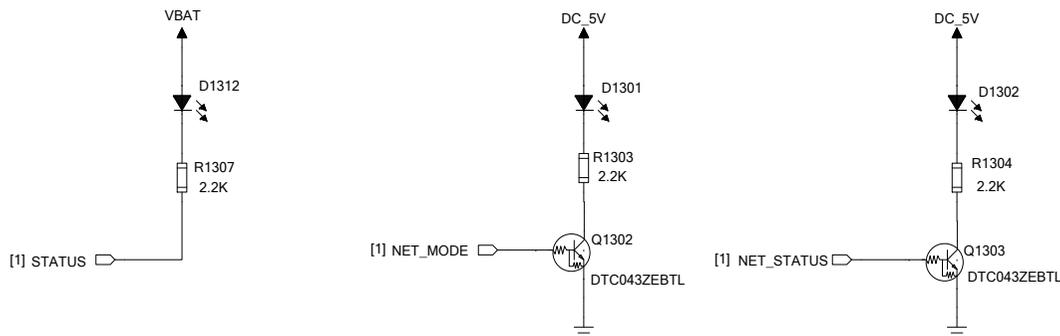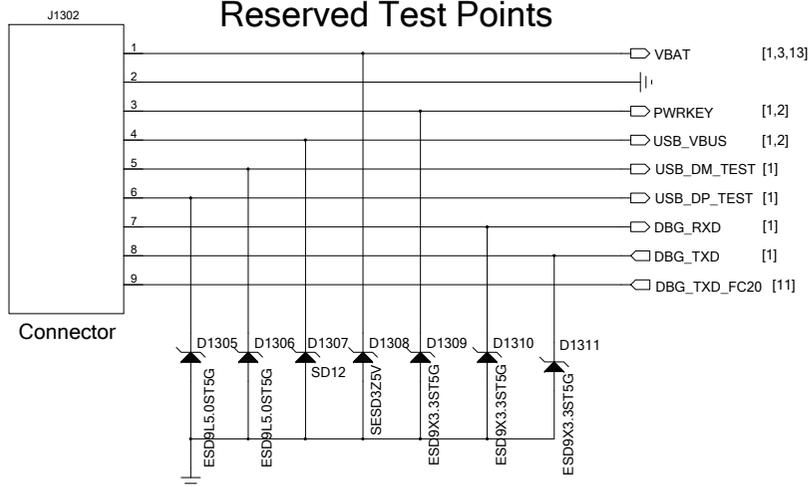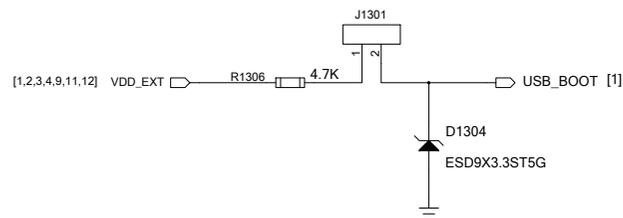
Notes:
1. The STATUS is an open drain output pin, and its drive current is less than 1mA.
2. For more details about NET_MODE and NET_STATUS, please refer to *Quectel_EC21_Hardware_Design.*
3. If the current consumption is required as low as possible when the device is in sleep, replace the power supply of indicators with controllable one.
   Turn off the power when the module enters into sleep mode.

Reserved Test Points

J1302

1	VBAT	[1,3,13]
2		
3	PWRKEY	[1,2]
4	USB_VBUS	[1,2]
5	USB_DM_TEST	[1]
6	USB_DP_TEST	[1]
7	DBG_RXD	[1]
8	DBG_TXD	[1]
9	DBG_TXD_FC20	[11]

Connector

D1305 D1306 D1307 D1308 D1309 D1310 D1311

ESD9L5.0ST5G ESD9L5.0ST5G SD12 SESD325V ESD9X3.3ST5G ESD9X3.3ST5G ESD9X3.3ST5G

Notes:
1. Both USB and debug UART interfaces are reserved for software debugging.
2. USB interface also can be used to upgrade firmware.
3. Junction capacitance of ESD protection devices on USB data lines should be less than 1pF.
4. The module DBG interface supports 1.8V power domain,
   A level translator should be used if the power domain of customers' application is 3.3V.

J1301

[1,2,3,4,9,11,12] VDD_EXT   R1306   4.7K   USB_BOOT [1]

D1304
ESD9X3.3ST5G

Notes:
1. It is recommended to reserve USB_BOOT design.
2. USB_BOOT is kept open by default.
   When it is at high level, the module will enter download mode.

Quectel Wireless Solutions		
DRAWN BY Lorry XU	PROJECT EC21	TITLE Reference Design
CHECKED BY Woody WU	SIZE A2	VER F
	SHEET 13OF 13	DATE 2018/2/9