EG912Y Series

Hardware Design

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Author	Description
1.0	2020-08-03	Claude WEI/ Niko WU/ Andrea ZHANG	Initial

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1 Introduction

This document defines Quectel's EG912Y series modules (hereinafter referred to as "EG912Y modules") and describes their air interfaces and hardware interfaces that are connected to your applications.

This document can help you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the EG912Y modules. To facilitate application of the EG912Y series modules to different fields, relevant reference designs are also provided here. Associated with application notes and user guides, you can use the EG912Y modules to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the EG912Y series modules. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, use emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as mobile phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.

2 Product Concept

2.1. General Description

The EG912Y modules refer to LTE-FDD/LTE-TDD/GSM wireless communication modules, and can provide data connectivity on LTE-FDD, LTE-TDD, EDGE and GPRS networks. The modules also provide voice functionality for your specific applications. Currently, the EG912Y series modules include 2 variants: EG912Y-CN and EG912Y-EU. The following table shows the frequency bands of the two modules.

Table 1: Frequency Bands of EG912Y-CN Module

Network Mode	Frequency Bands
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B34/B38/B39/B40/B41
GSM	900/1800 MHz

Table 2: Frequency Bands of EG912Y-EU Module

Network Mode	Frequency Bands
LTE-FDD	B1/B3/B5/B7/B8/B20/B28
LTE-TDD	B38/B40/B41
GSM	850/900/1800/1900 MHz

With a compact profile of 29.0 mm × 25.0 mm × 2.4 mm, the EG912Y modules can meet almost all requirements for M2M applications such as automotive field, smart metering, tracking system, security system, router, wireless POS, mobile computing device, PDA phone, tablet computer, etc.

The EG912Y modules are SMD type modules and they are embedded into applications through their 126 LGA pins.

2.2. Key Features

The following table shows the key features of the EG912Y series modules.

Table 3: Key Features of the EG912Y Series Modules

Feature	Details
Power Supply	Supply voltage: 3.4–4.5 V Typical supply voltage: 3.8 V
Transmitting Power	Class 4 (33 dBm ±2 dB) for EGSM900/GSM850 Class 1 (30 dBm ±2 dB) for DCS1800/PCS1900 Class E2 (27 dBm ±3 dB) for EGSM900/GSM850 8-PSK Class E2 (26 dBm ±3 dB) for DCS1800/PCS1900 8-PSK Class 3 (23 dBm ±2 dB) for LTE-FDD bands Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	Supports up to non-CA Cat 1 FDD and TDD Supports 1.4/3/5/10/15/20 MHz RF bandwidth FDD: Max 10 Mbps (DL), Max 5 Mbps (UL) TDD: Max 7.5 Mbps (DL), Max 1 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot Class 12 ● Coding scheme: CS-1, CS-2, CS-3 and CS-4 ● Max 85.6 kbps (DL), Max 85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot Class 12 ● Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1-9 ● Uplink coding schemes: MCS 1-9 ● Max 236.8 kbps (DL), Max 236.8 kbps (UL)
Internet Protocol Features	Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS/SMTP*/SMTPS* protocols Supports PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connection.
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast SMS storage: (U)SIM card currently
(U)SIM Interface	Supports USIM/SIM card: 1.8 V and 3.0 V Supports dual-card single-standby mode*

USB Interface	Complies with USB 2.0 specifications (slave mode only) in which the data transfer rate can theoretically reach up to 480 Mbps. Transmits data (including AT commands) and is used for debugging and upgrading software. Supports virtual USB serial drivers for Windows 7/8/8.1/10, Linux 2.6–5.4, Android 4.x/5.x/6.x/7.x/8.x/9.x, etc.
UART Interfaces	**Main UART:** ● Transmits data (including AT commands) ● Default Baud rate: 115200 bps ● Supports RTS and CTS hardware flow control. **Debug UART:** ● consoles Linux console and outputs logs ● Baud rate: 115200 bps
Audio Features	The module provides one analog input channel and one analog output channel.
PCM Interface*	provides audio function with an external codec. Supports 16-bit linear data format. Supports long frame synchronization and short frame synchronization. Supports master and slave modes. The master mode is necessary during long frame synchronization.
SPI Interface	Supports the master mode. Its operation voltage is 1.8 V with clock rates up to 52 MHz.
LCM Interface	Supports a maximum resolution of 240 × 320 LCD display module. Supports 4-line serial peripheral interface (SPI) and 1 lane SPI data transmission. Supports RGB565 format output.
Camera Interface	Supports 1-bit or 2-bit SPI interface.
WLAN Interface*	Supports SDIO 3.0 interface for WLAN.
AT Commands	Complies with 3GPP TS 27.007 and 27.005 commands and Quectel enhanced AT commands.
Network Indication	Pin NET_STATUS is configured to indicate network connectivity status.
Antenna Interfaces	Main antenna interface (ANT_MAIN) Characteristic impedance: 50 Ω
Physical Characteristics	Dimensions: (29.0 ±0.15) mm × (25.0 ±0.15) mm × (2.4 ±0.2) mm
Temperature Range	Operating temperature range: -35 °C to +75 °C [1)] Extended temperature range: -40 °C to +85 °C [2)] Storage temperature range: -40 °C to +90 °C
Software Upgrade	USB interface and FOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive.

NOTES

1. [1] Within the operating temperature range, the module meets 3GPP specifications.
2. [2] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network will not be influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module meets 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure is a block diagram of the EG912Y series modules. It illustrates the major functional parts.

- Power management
- Baseband
- Flash
- Radio frequency
- Peripheral interfaces

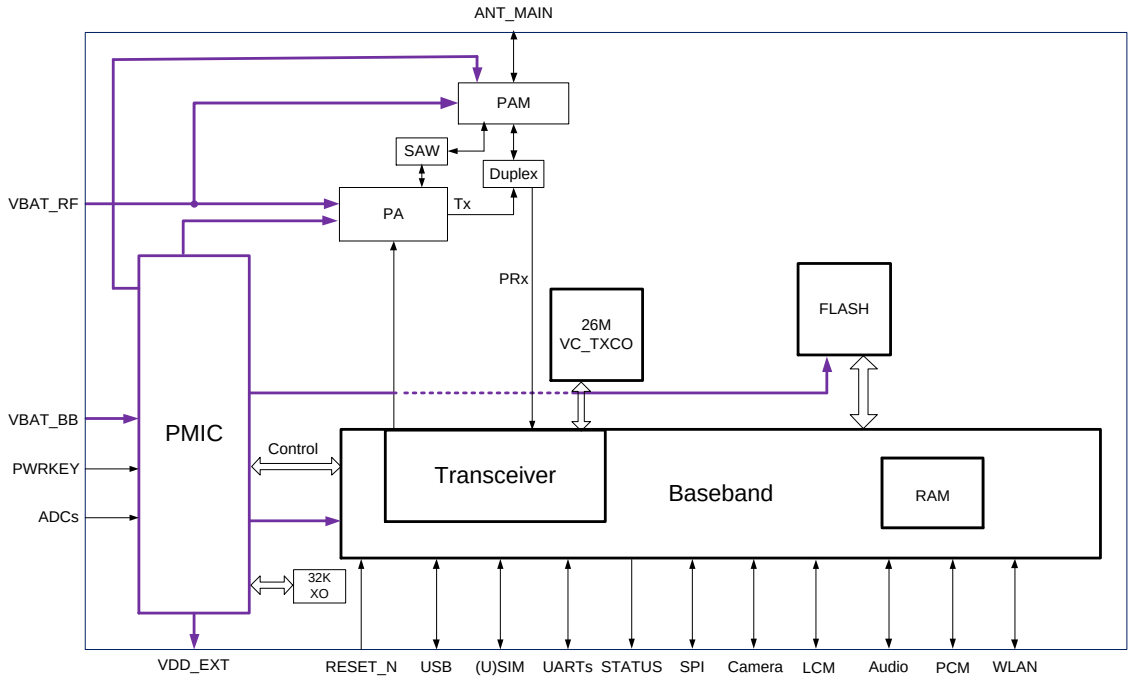


Figure 1: Functional Diagram

2.4. Evaluation Board

To develop optimal applications with the EG912Y series modules, Quectel provides an evaluation board (UMTS&LTE EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the modules better. For more details, see ***document [4]***.

3 Application Interfaces

3.1. General Description

The EG912Y series modules are equipped with 126 LGA pins that can be connected to cellular application platform. The subsequent chapters provide detailed descriptions of the following interfaces:

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- Audio interface
- PCM* and I2C interfaces
- Status indication
- SPI interface
- LCM interface
- Camera interface
- WLAN interface*
- ADC interface
- USB_BOOT interface
- Antenna interface

NOTE

"*" means under development.

3.2. Pin Assignment

The following figure shows the pin assignment of the EG912Y series modules.

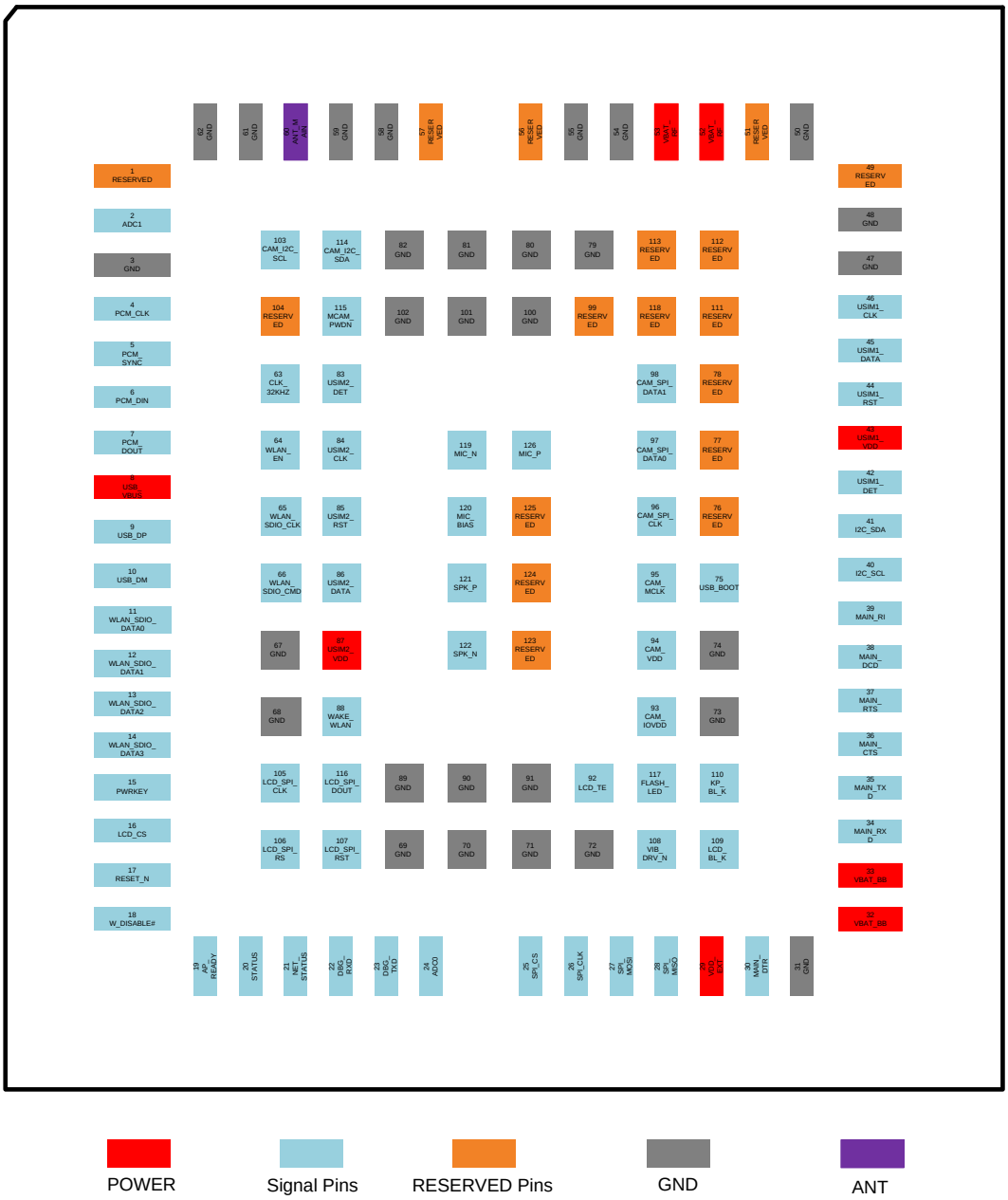


Figure 2: EG912Y Series Pin Assignment (Top View)

3.3. Pin Description

The following tables show the pin definition of EG912Y series.

Table 4: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32,33	PI	Power supply for the module's baseband part	Vmax = 4.5 V Vmin = 3.4 V Vnorm = 3.8 V	Current intensity needs to be no less than 0.8 A.
VBAT_RF	52,53	PI	Power supply for the module's RF part	Vmax = 4.5 V Vmin = 3.4 V Vnorm = 3.8 V	Current intensity needs to be no less than 2 A.
GND	3,31, 47,48, 50,54, 55,58, 59,61, 62, 67–74, 79–82, 89–91,		Ground		

	100–102				
Power Supply Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_EXT	29	PO	Provides 1.8 V for external circuits	Vnorm = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. If unused, keep this pin open.
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn-on/Turn-off key	V_{IL}max = 0.5 V	PWRKEY should be pulled down for a specified period to power on/off the system.
RESET_N	17	DI	Resets the module Active low	V_{IL}max = 0.5 V	If unused, keep this pin open.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicates the module's operating status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep this pin open.
NET_ STATUS	21	DO	Indicates the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep this pin open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	PI	Detects USB	Vmax = 5.25 V Vmin = 3.0 V Vnorm = 5.0 V	Typical voltage: 5.0 V If unused, keep this pin open.
USB_DP	9	IO	USB differential data bus (+)	Complies with USB 2.0 standard specifications.	Requires differential impedance of 90 Ω. If unused, keep this pin open.
USB_DM	10	IO	USB differential data bus (-)	Complies with USB 2.0 standard	Requires differential impedance of 90 Ω.

				specifications.	If unused, keep this pin open.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	43	PO	Power supply for (U)SIM1 card	Iomax = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_RST	44	DO	Reset signal of (U)SIM1 card	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_DATA	45	IO	Data signal of (U)SIM1 card	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_CLK	46	DO	Clock signal of (U)SIM1 card	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_DET	42	DI	(U)SIM1 card insertion detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
USIM2_VDD	87	PO	Power supply for (U)SIM2 card	Iomax = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:**	Either 1.8 V or 3.0 V is supported by the module automatically.

				Vmax = 3.05 V Vmin = 2.7 V	
USIM2_RST	85	DO	Reset signal of (U)SIM2 card	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_DATA	86	IO	Data signal of (U)SIM2 card	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_CLK	84	DO	Clock signal of (U)SIM2 card	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_DET	83	DI	(U)SIM2 card insertion detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	30	DI	Data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
MAIN_RXD	34	DI	Receives data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
MAIN_TXD	35	DO	Transmits data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.

MAIN_CTS	36	DO	Main UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
MAIN_RTS	37	DI	Main UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
MAIN_DCD	38	DO	Data carrier detection	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
MAIN_RI	39	DO	Ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Receives data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
DBG_TXD	23	DO	Transmits data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose analog-to-digital converter	Voltage range: 0 V–VBAT_BB	If unused, keep this pin open.
ADC1	2	AI	General-purpose analog-to-digital converter	Voltage range: 0 V–VBAT_BB	If unused, keep this pin open.
Audio Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_BIAS	120	PO	Bias voltage output for microphone		If unused, keep this pin open.
MIC_N	119	AI	Microphone analog input (-)		If unused, keep this pin open.
MIC_P	126	AI	Microphone analog input (+)		

SPK_P	121	AO	Analog audio differential output (+)		Internal reactive power amplifier. This interface can be used to drive external power amplifier devices. If unused, keep this pin open.
SPK_N	122	AO	Analog audio differential output (-)		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	4	DO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
PCM_SYNC	5	DO	PCM data frame synchronization	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
PCM_DIN	6	DI	Inputs PCM data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
PCM_DOUT	7	DO	Outputs PCM data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	40	OD	I2C serial clock. Used for external codec.		An external 1.8 V pull-up resistor is required. If unused, keep this pin open.
I2C_SDA	41	OD	I2C serial data. Used for external codec.		An external 1.8 V pull-up resistor is required. If unused, keep this pin open.
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CAM_IOVDD	93	PO	Camera IO power	Vnorm = 1.8 V	1.8 V power domain. If unused, keep this pin open.
CAM_VDD	94	PO	Camera power	Vnorm = 2.8 V	If unused, keep this pin

					open.
CAM_MCLK	95	DO	Camera clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
CAM_SPI_CLK	96	DI	Camera SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
CAM_SPI_DATA0	97	DI	Camera SPI data inputs 0 data bit	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
CAM_SPI_DATA1	98	DI	Camera SPI data inputs 1 data bit	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
CAM_I2C_SCL	103	OD	Camera I2C clock		1.8 V power domain. If unused, keep this pin open.
CAM_I2C_SDA	114	OD	Camera I2C data		1.8 V power domain. If unused, keep this pin open.
MCAM_PWDN	115	DO	Camera off	V_{OL}max = 0.45V V_{OH}min = 1.35V	1.8 V power domain. If unused, keep this pin open.
FLASH_LED	117	OD	Drives Flash/Flashlight output		Sink current drive, adjustable within the maximum 64 mA. If unused, keep this pin open.
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_CS	16	DO	LCD CS	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
LCD_TE	92	DI	LCD tearing effect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
LCD_SPI_CLK	105	DO	LCD SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.

LCD_SPI_RS	106	DO	Selects LCD Register	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
LCD_SPI_RST	107	DO	Resets LCD SPI	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
LCD_BL_K	109	OD	LCD backlight driver		Sink current drive, adjustable within the maximum 96 mA. If unused, keep this pin open.
LCD_SPI_DOUT	116	DO	Outputs LCD SPI data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
WLAN Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SDIO_DATA0	11	IO	WLAN SDIO data bus D0	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
WLAN_SDIO_DATA1	12	IO	WLAN SDIO data bus D1	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
WLAN_SDIO_DATA2	13	IO	WLAN SDIO data bus D2	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
WLAN_SDIO_DATA3	14	IO	WLAN SDIO data bus D3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
WLAN_EN	64	DO	Enables controlling WLAN	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin

					open.
WLAN_SDIO_CLK	65	DO	WLAN SDIO bus clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
WLAN_SDIO_CMD	66	DO	WLAN SDIO bus command	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
WLAN_WAKE	88	DI	Wakes up the host (EG912Y series modules) via an external Wi-Fi module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	25	DO	SPI CS	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
SPI_CLK	26	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
SPI_MOSI	27	DO	SPI MOSI	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
SPI_MISO	28	DI	SPI MISO	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	IO	Main antenna		50 Ω impedance.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AP_READY	19	DI	Detects application processor sleep state	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
W_	18	DI	Controls the	V_{IL}min = -0.3 V	1.8 V power domain.

DISABLE#			airplane mode	V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	Pull-up by default. In a low voltage level, the module can enter the airplane mode. If unused, keep this pin open.
CLK_32KHZ	63	DO	Outputs 32 kHZ clock signal		If unused, keep this pin open.
KP_BL_K	110	OD	Drives key backlight		Sink current drive, adjustable within the maximum 64 mA,. If unused, keep this pin open.
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	75	DI	Forces the module to enter emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Active high. It is recommended to reserve it as a test point.
Motor interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIB_DRV_N	108	OD	Controls the motor drive		
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	1, 49,51, 56,57, 76–78, 99, 104, 111–113 118, 123–125		Reserved		Keep these pins open.

3.4. Operating Modes

The table below summarizes the various operating modes mentioned in the following chapters.

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The modules have registered on network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rates.
Minimum Functionality Mode	The **AT+CFUN=0** command sets the module to a minimum functionality mode without removing the power supply. In this case, both RF and (U)SIM card functions are invalid.	
Airplane Mode	The **AT+CFUN=4** command or the W_DISABLE# pin sets the modules to enter the airplane mode. In this mode, RF function is unavailable.	
Sleep Mode	In this mode, the current consumption of the modules is reduced to the minimal level. The module still receives paging messages, SMS, voice calls and TCP/UDP data from the network.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

The EG912Y series modules reduce their power consumption to a minimum value in the sleep mode. The following sub-chapters describe the power saving procedures of the EG912Y series modules.

3.5.1.1. UART Application

If a host (a user's device) communicates with the modules via the UART interface, You can make the module enter the sleep module with either of the following methods.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Drive MAIN_DTR to the high level or keep it open.

The following figure shows the connection between the module and the host.

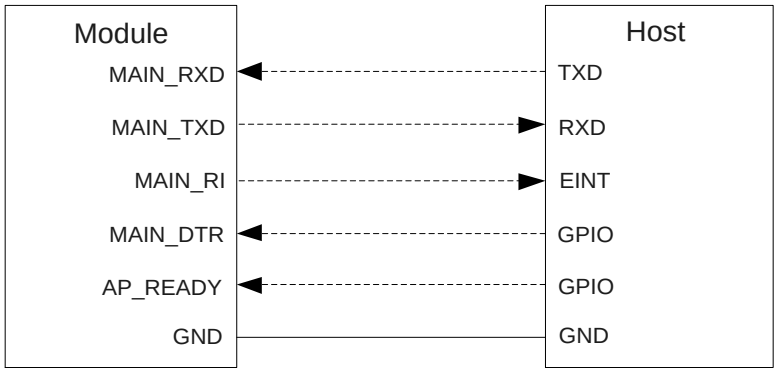


Figure 3: Sleep Mode Application via UART

Driving the host MAIN_DTR to the low level wakes up the module.

- To report a URC, MAIN_RI signal wakes up the host. See ***Chapter 3.21*** for details about MAIN_RI behavior.
- AP_READY detects the sleep state of the host (The AP_READY pin is configurable to high level or low level detection). See **AT+QCFG="apready"*** in ***document [2]*** for details.

3.5.1.2. USB Application with Remote Wakeup Function

If the host supports suspending/resuming USB and USB remote wakeup functions, the following three preconditions must be met to make the modules enter the sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- The MAIN_DTR pin is held at high level or keep it open.
- The host's USB, which is connected to the module's USB interface, enters the suspension state.

The following figure shows the connection between the module and the host.

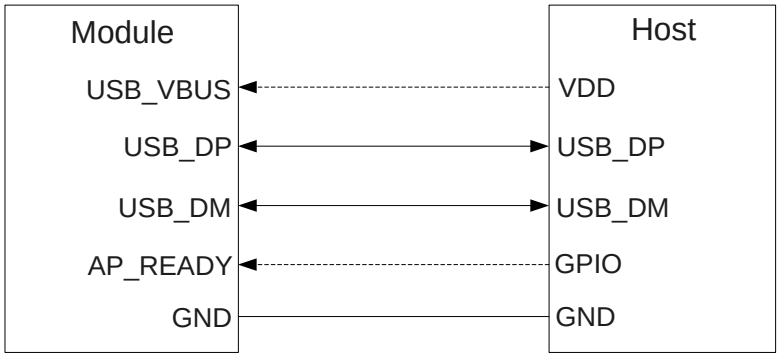


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module via USB wakes up the module.
- To report a URC, the module sends remote wakeup signals via the USB cable to wake up the host.

3.5.1.3. USB Application with USB Suspension/Resuming and MAIN_RI Functions

If the host supports suspending/resuming USB, but does not support USB remote wake-up function, the MAIN_RI signal is needed to wake up the host.

The following three preconditions must be met to make the module enter the sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure that the MAIN_DTR pin is held at high level or keep it open.
- The host's USB, which is connected to the module's USB interface, enters the suspension state.

The following figure shows the connection between the module and the host.

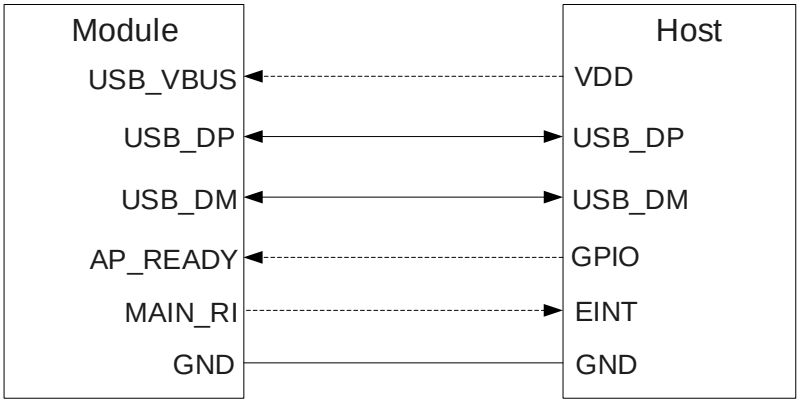


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to the module via USB wakes up the module.
- To report a URC, MAIN_RI signal wakes up the host.

3.5.1.4. USB Application without USB Suspension Function

If the host does not support the USB suspension function, disconnect USB_VBUS with an external control circuit to let the modules enter sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure that the MAIN_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure illustrates the connection between the module and the host.

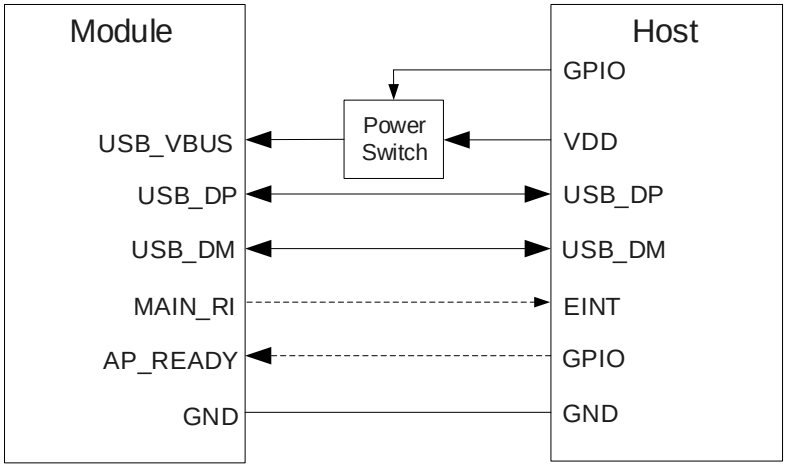


Figure 6: Sleep Mode Application without Suspension Function

Switching on the power to supply power for USB_VBUS wakes up the module.

NOTE

Pay attention to the level matching shown by dotted lines between the module and the host. See ***document [1]*** for more details about the power management application of the EG912Y series modules.

3.5.2. Airplane Mode

When the module is in the airplane mode, the RF function does not work, and all AT commands correlative with RF function are inaccessible.

You can set the module into this mode by the following ways.

Hardware:

Drive Pin W_DISABLE# to the low level to let the module enter the airplane mode. The W_DISABLE# pin is pulled up by default.

Software:

AT+CFUN=<fun> command provides the choice of the functionality level through setting **<fun>** as 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTE

Controlling the airplane mode via the W_DISABLE# pin is disabled in firmware by default. It can be enabled by the **AT+QCFG="airplanecontrol",1** command and this command is under development.

3.6. Power Supply

3.6.1. Power Supply Pins

The EG912Y series modules provide VBAT pins for connection with an external power supply. There are two separate voltage domains for VBAT.

- VBAT_RF pins supplies power for the module's RF part.
- VBAT_BB pins supplies power for the module's baseband part.

The following table shows the details of VBAT and ground pins.

Table 7: Pin Definition of VBAT and GND

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52,53	Power supply for the module's RF part.	3.4	3.8	4.5	V
VBAT_BB	32,33	Power supply for the module's baseband part.	3.4	3.8	4.5	V
GND	3,31,	Ground	-	0	-	V

	47,48, 50,54, 55,58, 59,61, 62, 67–74, 79–82, 89–91, 100–102

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.4 V to 4.5 V. Make sure that the input voltage never drops below 3.4 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drops are less in 3G and 4G networks than that in the 2G's.

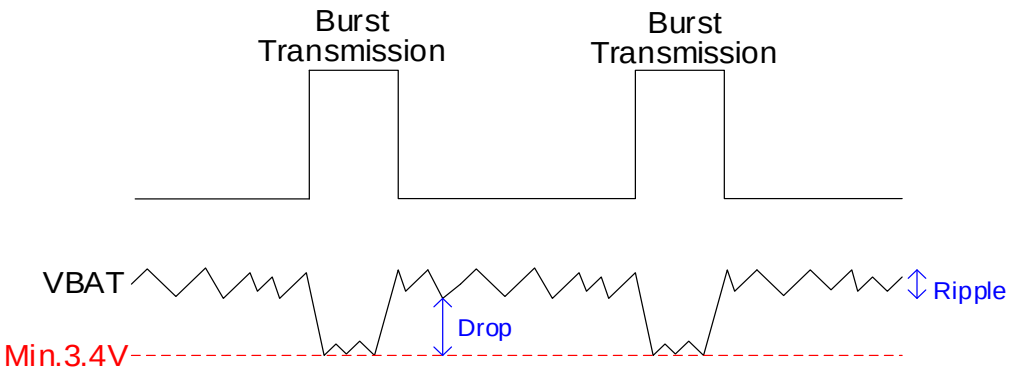


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, use a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω), and reserve a multi-layer ceramic chip (MLCC) capacitor array due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single-voltage source. Route VBAT_BB and VBAT_RF traces to two sub paths in a star structure. The width of the VBAT_BB trace should be no less than 1 mm, and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it is.

In addition, to avoid the damage caused by electric surge and ESD, you can use a TVS diode with low reverse stand-off voltage (V_{RWM} = 4.7 V), low clamping voltage (V_C) and high reverse peak pulse current (I_{PP}) should be used. The following figure shows the star structure of the power supply.

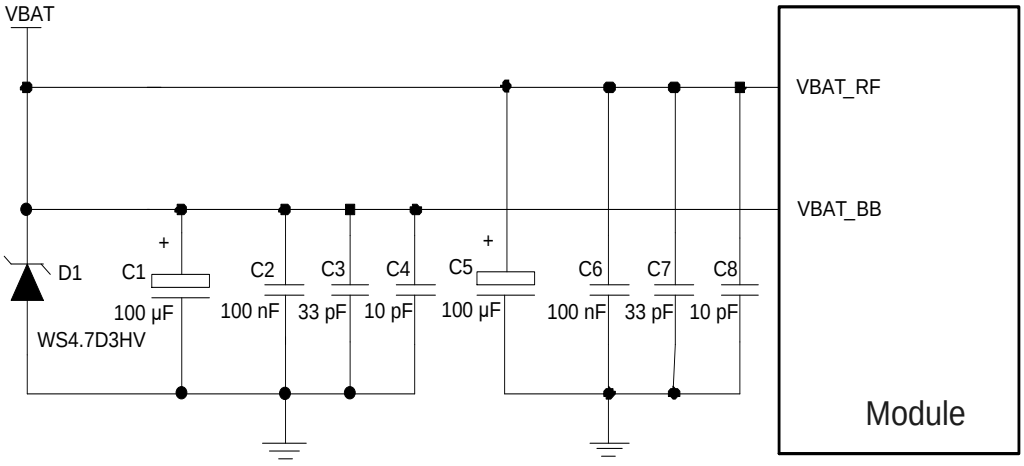


Figure 8: Star Structure of Power Supply

3.6.3. Reference Design for Power Supply

The power design of a module is very important, as the module's performance largely depends on the power source. For the EG912Y series modules, the power supply should be able to provide sufficient current up to 3 A at least. If the voltage drop between the input and output is not too high, you can use an LDO to supply power for the modules. If there is a big voltage difference between the input source and the desired output (VBAT), preferably use a buck converter as the power supply.

The following figure shows a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

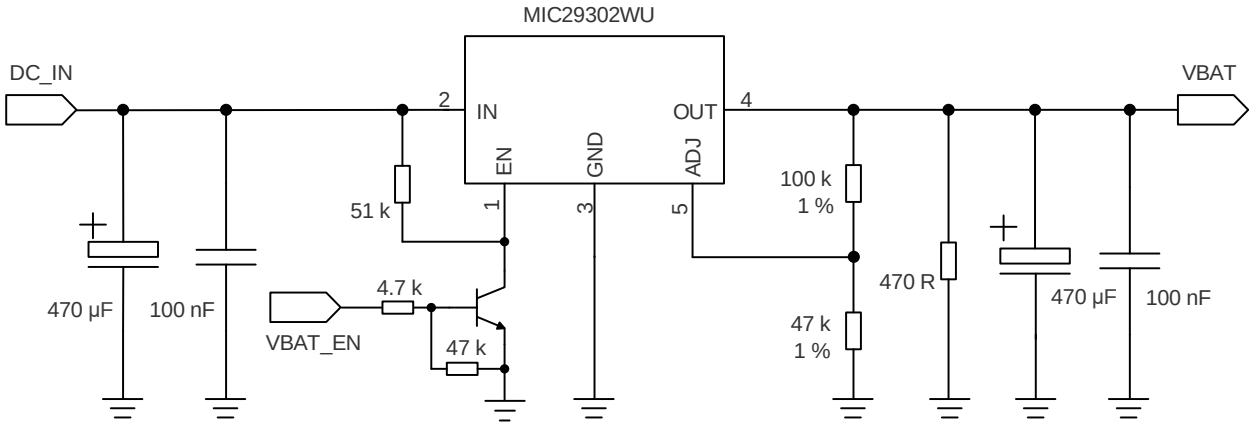


Figure 9: Reference Circuit of Power Supply

3.6.4. Monitor the Power Supply*

You can use the **AT+CBC** command to monitor the VBAT_BB voltage value. For more details, see ***document [2]***.

NOTE

"*" means under development.

3.7. Power-on/off Scenarios

3.7.1. Turn on the Module by Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	15	Turn-on/Turn-off key.	V_{IL}max = 0.5 V	Pull down PWRKEY for 500 ms to power on/off the system.

When a EG912Y module is turned off, you can turn on the module by driving the PWRKEY pin to the low level for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After the STATUS pin outputting a high level voltage, release the PWRKEY pin . A simple reference circuit is illustrated in the following figure.

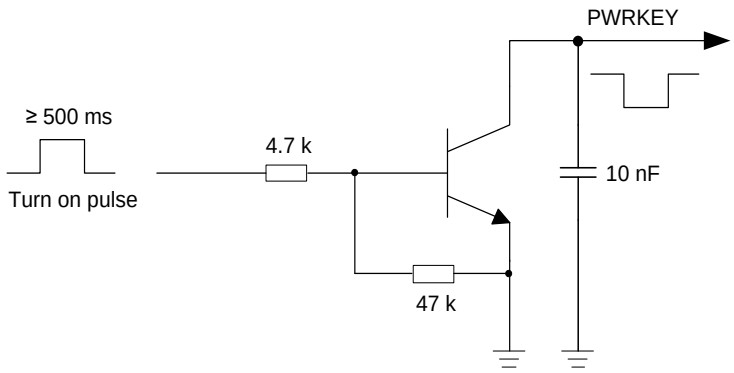


Figure 10: Turn on the Module Using the Driving Circuit

You can also control the PWRKEY pin by adding a button for the pin directly. Place a TVS component nearby the button for ESD protection. A reference circuit is shown in the following figure.

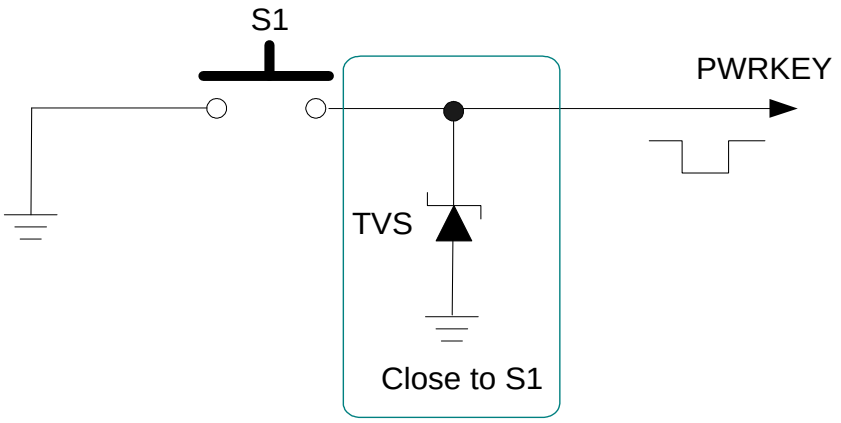


Figure 11: Turn on the Module Using the Button

The power-on scenario is illustrated in the following figure.

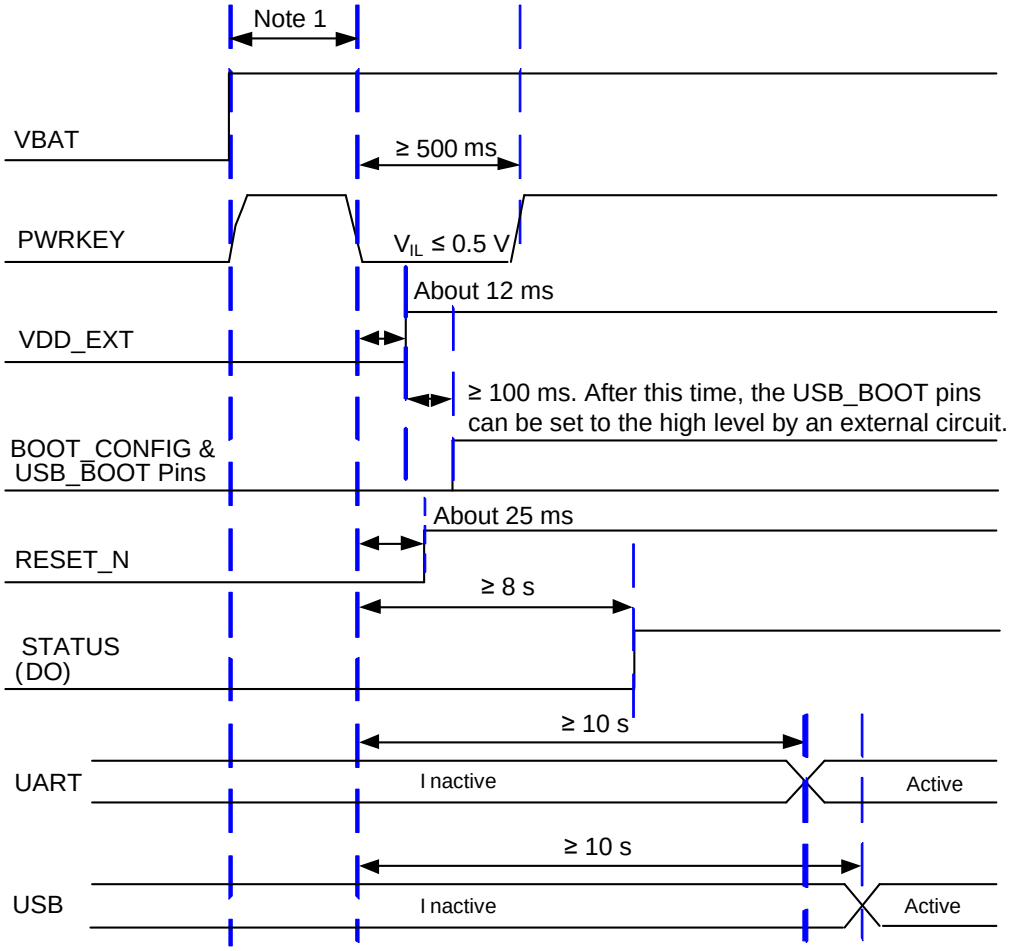


Figure 12: Timing of Turning on the Module

NOTES

1. Make sure that VBAT is stable before pulling down the PWRKEY pin. The time between supplying power from the VBAT pins and pulling down the PWRKEY pin is no less than 30 ms.
2. You can pull down the PWRKEY pin directly to GND with a 1 kΩ resistor if the module needs to be powered on automatically without shutdown.

3.7.2. Turn off the Module

You can use the following two methods to turn off the module:

- Turn off the module by using the PWRKEY pin.
- Turn off the module by using the **AT+QPOWD** command.

3.7.2.1. Turn off the Module by Using the PWRKEY Pin

Drive the PWRKEY pin to the low level voltage for at least 600 ms. The module executes power-off procedure after the PWRKEY pin is released. The power-off scenario is illustrated in the following figure.

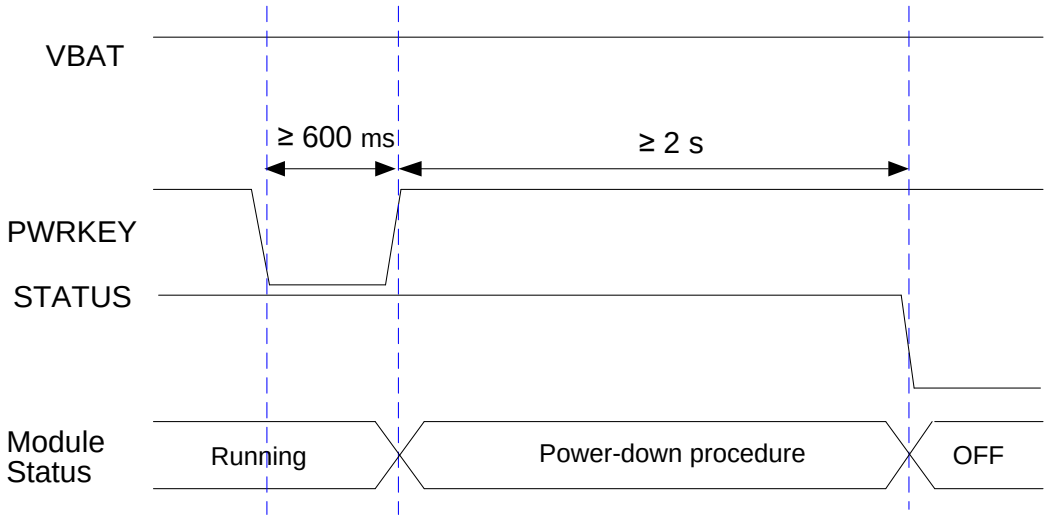


Figure 13: Timing of Turning off Module

3.7.2.2. Turn off Module by Using AT Command

You can also use the AT+QPOWD command to turn off the module. See ***document [2]*** for details about the **AT+QPOWD** command.

NOTES

1. To avoid damaging the internal flash, do NOT switch off the power supply when the module works normally. Only after the module is shut down by the PWRKEY pin or the AT command can the power supply be cut off.
2. When using the AT command to turn off the module, keep the PWRKEY pin at the high level after the execution of the power-off command. Otherwise, the module will turn on again after being turned off.

3.8. Reset the Module

You can use the RESET_N pin to reset the module. To reset it, drive RESET_N to a low level voltage for at least 300 ms. The RESET_N pin's signal is sensitive to interference. Therefore, route the trace of the pin as short as possible and protect the trace with signal grounding.

Table 9: Pin Definition of RESET_N

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	17	Resets the module Active low	V_{IL}max = 0.5 V	If unused, keep it open.

The recommended circuit for the RESET_N pin is similar to the reference circuit for the PWRKEY pin. You can use an open drain/collector driver or button to control the RESET_N pin.

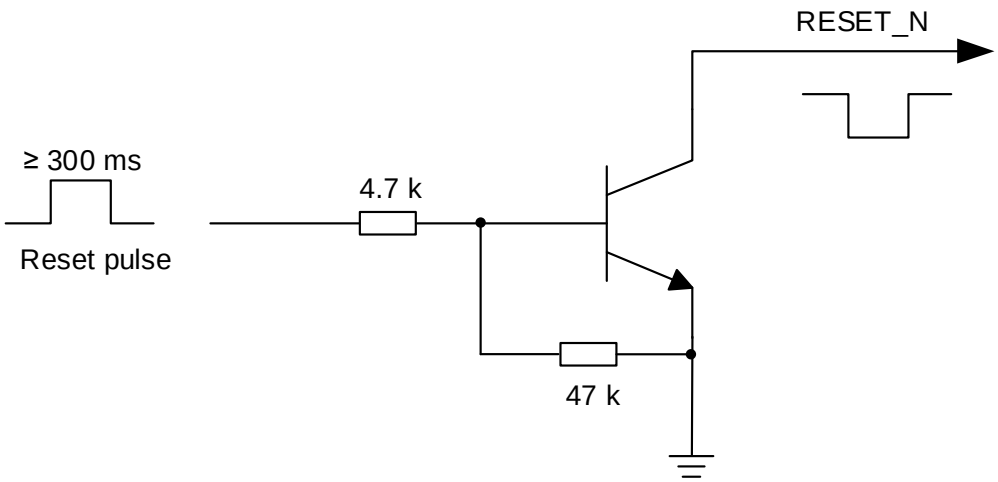


Figure 14: Reference Circuit of RESET_N by Using the Driving Circuit

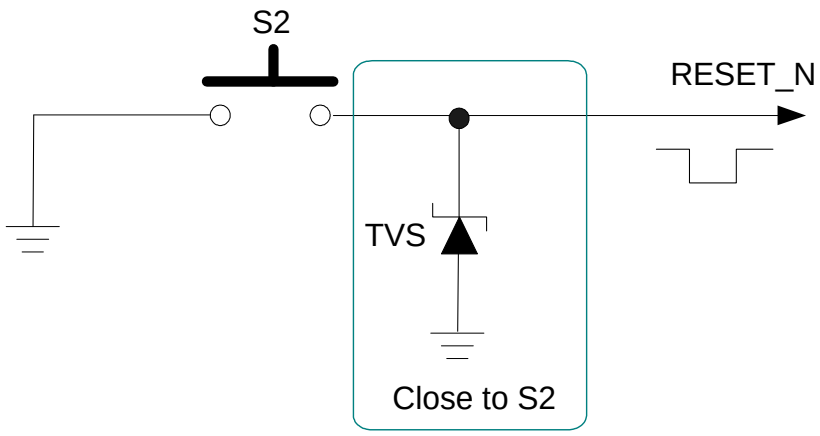


Figure 15: Reference Circuit of RESET_N by Using the Button

The reset scenario is illustrated in the following figure.

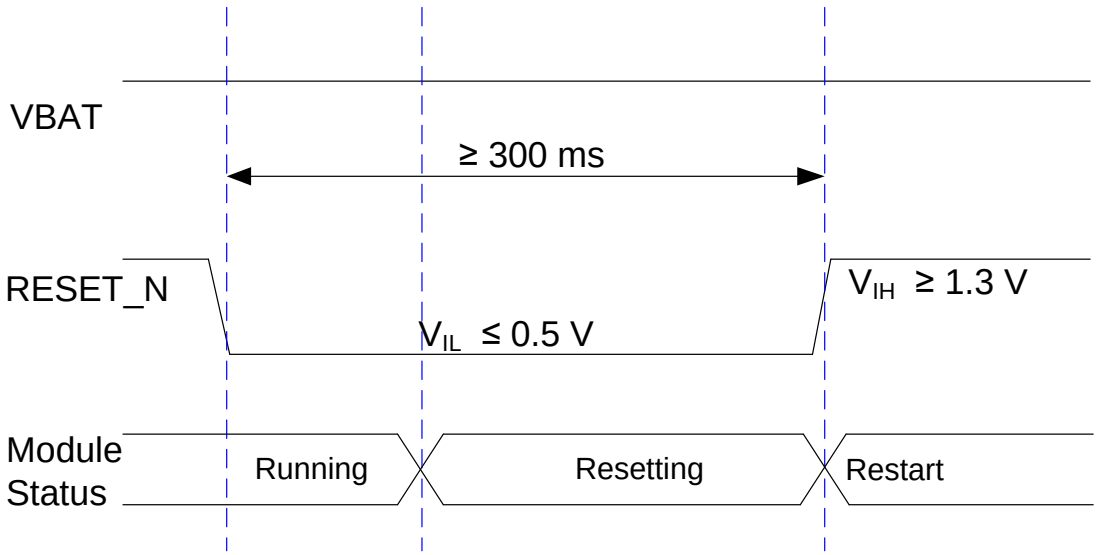


Figure 16: Timing of Resetting the Module

NOTES

1. Ensure that there is no large capacitance on the PWRKEY and RESET_N pins. The capacitance cannot exceed 10 nF.
2. The RESET_N pin resets the baseband chip of the modules. It does not reset the chip of power management.
3. Reset the module only when the module fails to be turned off by the **AT+QPOWD** command or the PWRKEY pin.

3.9. (U)SIM Interfaces

The EG912Y series modules provide two (U)SIM interfaces. The (U)SIM interfaces circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported. The modules also support dual-card single-standby function*.

The following table shows the pin definition of the (U)SIM interfaces.

Table 10: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	Power supply for (U)SIM1 card	The modules identify 1.8 V or 3.0 V (U)SIM1 cards automatically.
USIM1_RST	44	DO	Reset signal of (U)SIM1 card	
USIM1_DATA	45	IO	Data signal of (U)SIM1 card	
USIM1_CLK	46	DO	Clock signal of (U)SIM1 card	
USIM1_DET	42	DI	(U)SIM1 card insertion detection	1.8 V power domain. If unused, keep this pin open.
USIM2_VDD	87	PO	Power supply for (U)SIM2 card	The modules identify 1.8 V or 3.0 V (U)SIM1 cards automatically.
USIM2_RST	85	DO	Reset signal of (U)SIM2 card	
USIM2_DATA	86	IO	Data signal of (U)SIM2 card	
USIM2_CLK	84	DO	Clock signal of (U)SIM2 card	
USIM2_DET	83	DI	(U)SIM2 card insertion detection	1.8 V power domain. If unused, keep this pin open.

The following figure illustrates a reference design for the (U)SIM interface with an 8-pin (U)SIM card connector.

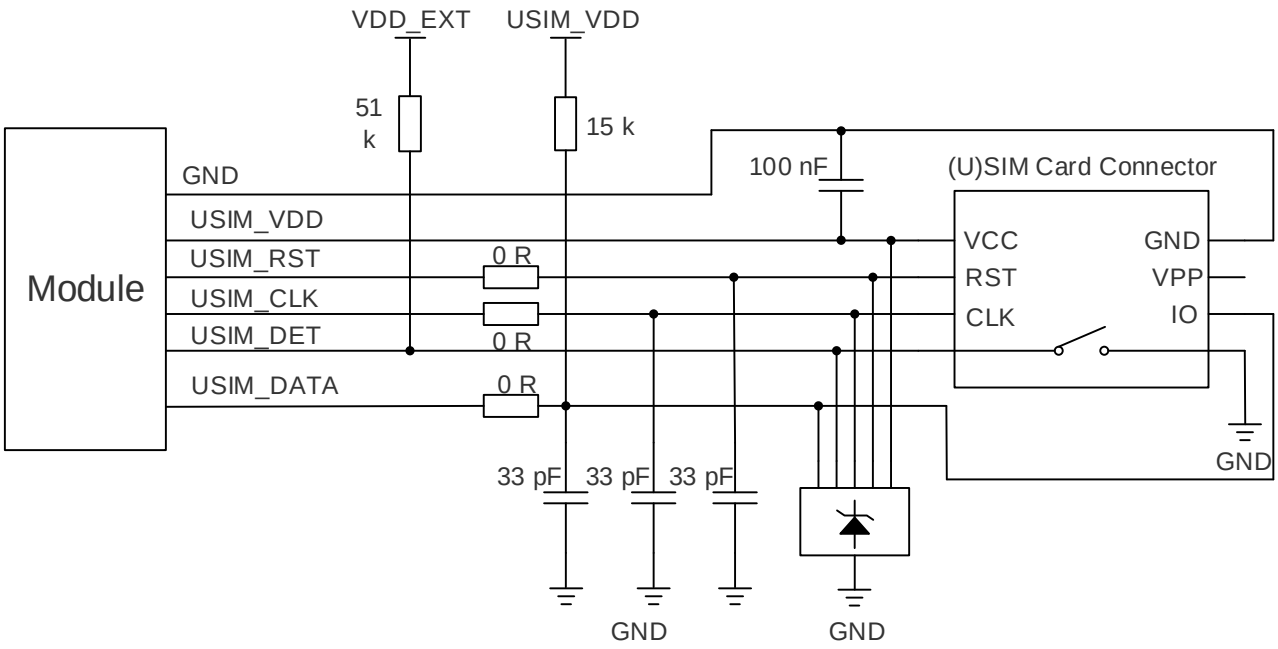


Figure 17: Reference Circuit of the (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET disconnected. A reference circuit of the (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

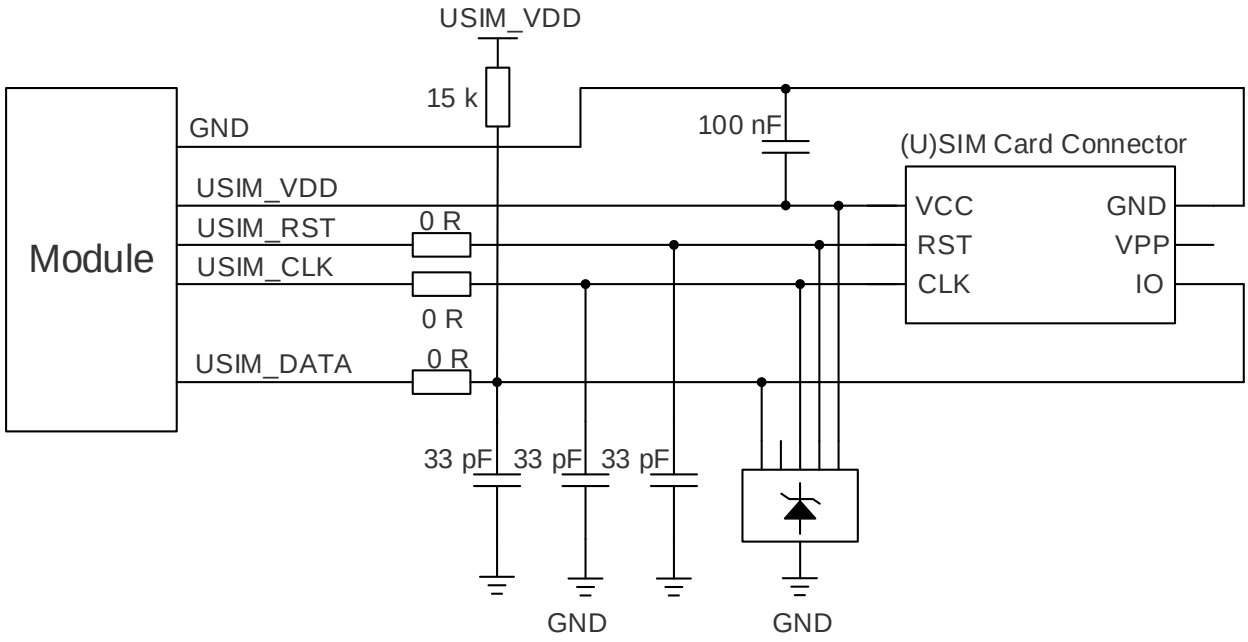


Figure 18: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM cards in your applications, follow the criteria below in designing the (U)SIM circuits:

- Keep placement of the (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Make sure the bypass capacitor between USIM_VDD and GND less than 1 μF, and place it as close to the (U)SIM card connector as possible.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability. When long layout traces and sensitive occasions are applied, it should be placed close to the (U)SIM card connector.

NOTE

"*" means under development.

3.10. USB Interface

The EG912Y series modules contain one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface acts as slave only, and is used for transmitting data (including AT commands), debugging and upgrading software.
The following table shows the pin definition of USB interface.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	PI	USB connection detection	Typical: 5.0 V
USB_DP	9	IO	USB differential data bus (+)	Requires differential impedance of 90 Ω.
USB_DM	10	IO	USB differential data bus (-)	Requires differential impedance of 90 Ω.

For more details about USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware debugging and upgrade in your design. The following figure shows a reference circuit of USB interface.

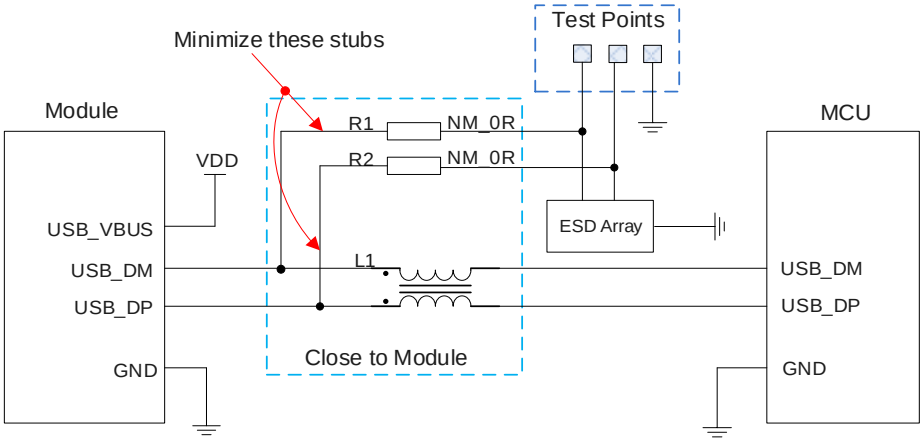


Figure 19: Reference Circuit of the USB Interface

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data line signal, place L1/R1/R2 components close to the module, and place these resistors close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with in designing the USB interface to meet the USB 2.0 specifications.

- Route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Do NOT route signal traces under crystals, oscillators, magnetic devices and RF signal traces. Route the USB differential traces in the inner-layer of the PCB with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of the junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2 pF.
- Keep the ESD protection components to the USB connector as close as possible.

3.11. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. This section introduces their features.

- The main UART interface supports 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600 bps baud rates, and the default baud rate is 115200 bps. It supports RTS and CTS hardware

flow control, and it is used for transmitting data (including AT commands).

- The debug UART interface supports 115200 bps baud rate. It is used for consoling Linux and outputting log output.

The following tables shows the pin definition of the two UART interfaces.

Table 12: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	30	DI	Data terminal ready	1.8 V power domain
MAIN_RXD	34	DI	Receives data	
MAIN_TXD	35	DO	Transmits data	
MAIN_CTS	36	DO	Main UART clear to send	
MAIN_RTS	37	DI	Main UART request to send	
MAIN_DCD	38	DO	Data carrier detection	
MAIN_RI	39	DO	Ring indication	

Table 13: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Receives data	1.8 V power domain
DBG_TXD	23	DO	Transmits data	1.8 V power domain

The logic levels of digital I/O of the interface are described in the following table.

Table 14: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V

V_{OH}	1.35	1.8	V

The module provides 1.8 V UART interfaces. Use a level translator if 'your application is equipped with a 3.3 V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure illustrates a reference design.

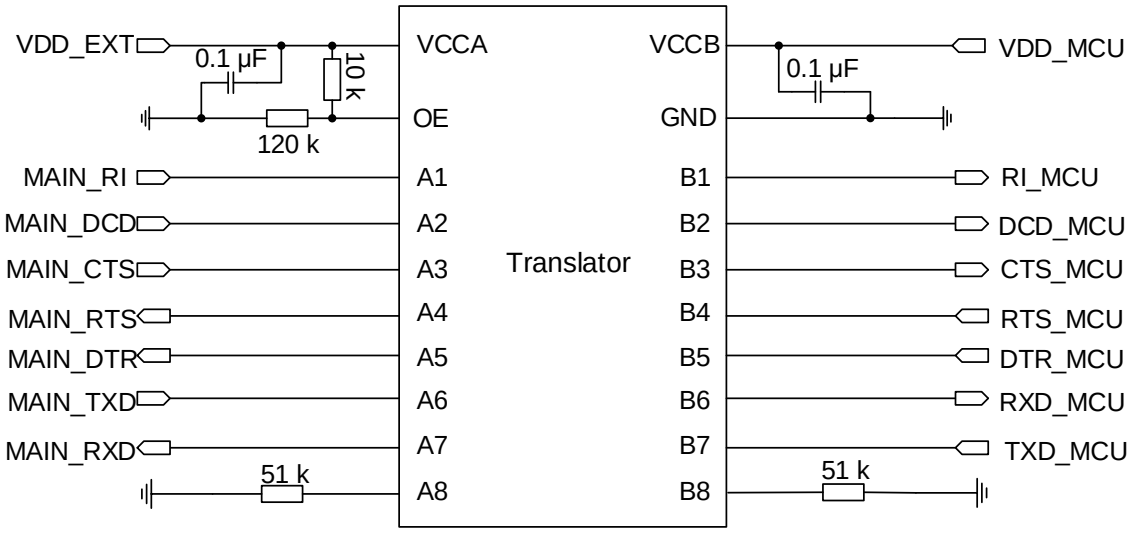


Figure 20: Reference Circuit with Translator Chip

Visit http://www.ti.com for more information.

The following figure shows another example of the transistor translation circuit. For the module's input and output circuit designs illustrated by dotted lines, you can refer to the circuit design in solid lines. Pay attention to the direction of connection.

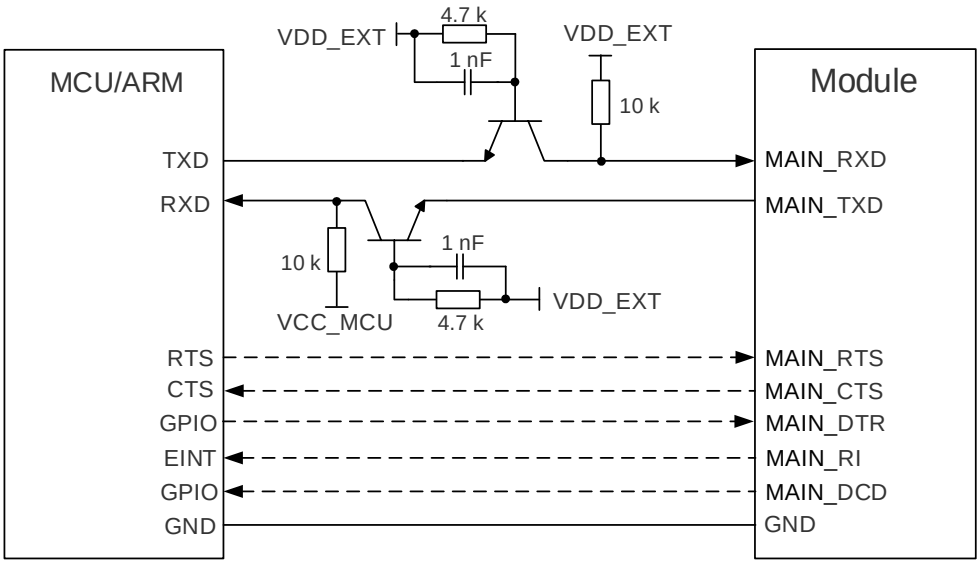


Figure 21: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.

3.12. Audio Interface

The module provides one analog input channel and one analog output channel.

Table 15: Pin Definition of Audio Interface

Pin Name	Pin No.	I/O	Description	Comment
MIC_BIAS	120	PO	Bias voltage output for microphone	If unused, keep this pin open.
MIC_N	119	AI	Microphone analog input (-)	If unused, keep this pin open.
MIC_P	126	AI	Microphone analog input (+)	
SPK_P	121	AO	Analog audio differential output (+)	Internal reactive power amplifier, this interface can be used to drive external power amplifier devices. If unused, keep this pin open.
SPK_N	122	AO	Analog audio differential output (-)	

You can use the audio input channel as the microphone of your application. An electret microphone is usually used. The audio input channel are differential input channels.

You can use the audio output channel as the earpiece or speaker (requires external audio amplifier) output for your application. The audio output channel supports voice and ringtone output functions.

For each channel, you can use the following commands:

- **AT+QMIC***:Adjust the input gain level of the microphone.
- **AT+CLVL***: Adjust the output gain level of the receiver and speaker.
- **AT+QSIDET***: Sets the side-tone gain level.

For more details of the commands, see ***document [2]***.

NOTE

"*" means under development.

3.12.1. Decrease TDD Noise and other Noise

You can use built-in RF filter dual capacitance microphones (e.g. 10 pF and 33 pF) to filter out RF interference from the source and greatly reduce coupled TDD noise. The 33 pF capacitor is applied for filtering out 900 MHz RF interference when the module is transmitting at EGSM900. Without this capacitor, TDD noise could be heard. Meanwhile, the 10 pF capacitor here is for filtering out 1800 MHz RF interference. However, the resonant frequency point of a capacitor largely depends on the material and production technique of the capacitor. Therefore, you may ask your capacitor vendors' suggestion for choosing the most suitable capacitor for filtering out EGSM900 and DCS1800 separately.

The severity degree of the RF interference in the voice channel during GSM transmitting period largely depends on your application design. In some cases, the EGSM900 TDD noise is more severe than the DCS1800 TDD noise; while in other cases, the DCS1800 TDD noise is more obvious. Therefore, you can choose your RF filtering on the base of test results. Sometimes, even no RF filtering capacitor is required.

The capacitor used for filtering out RF noise should be close to the audio interface or other audio interfaces. Audio alignment should be as short as possible.

To decrease radio or other signal interference, keep your RF antenna away from the audio interface and audio alignment. Do not parallel your power alignment to the audio alignment. Keep the power alignment far away from the audio alignment.

Route the differential audio traces according to the differential signal layout rule.

3.12.2. Microphone Interfaces Design

A reference circuit is shown in the following figure.

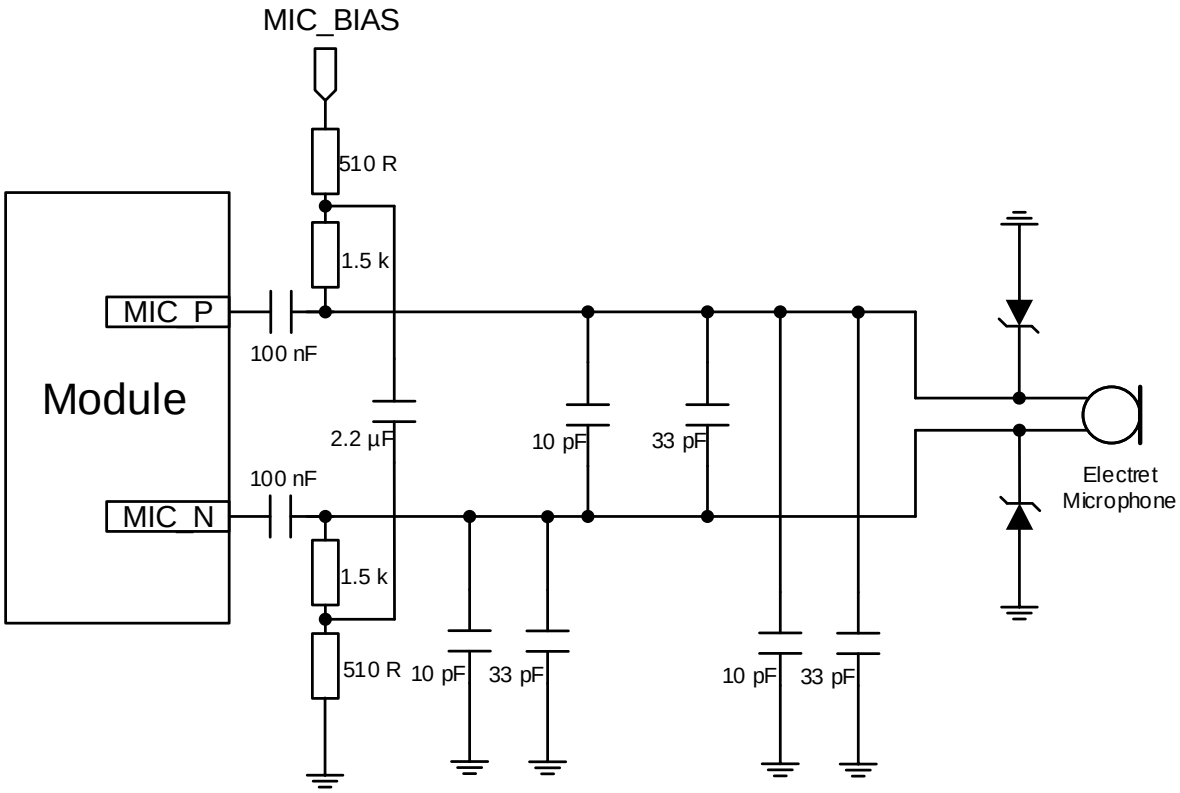


Figure 22: Reference Design for Audio input

NOTE

Since the microphone channel is sensitive to ESD, do NOT remove the ESD protection device of the microphone channel.

3.12.3. Receiver and Speaker Interface Design

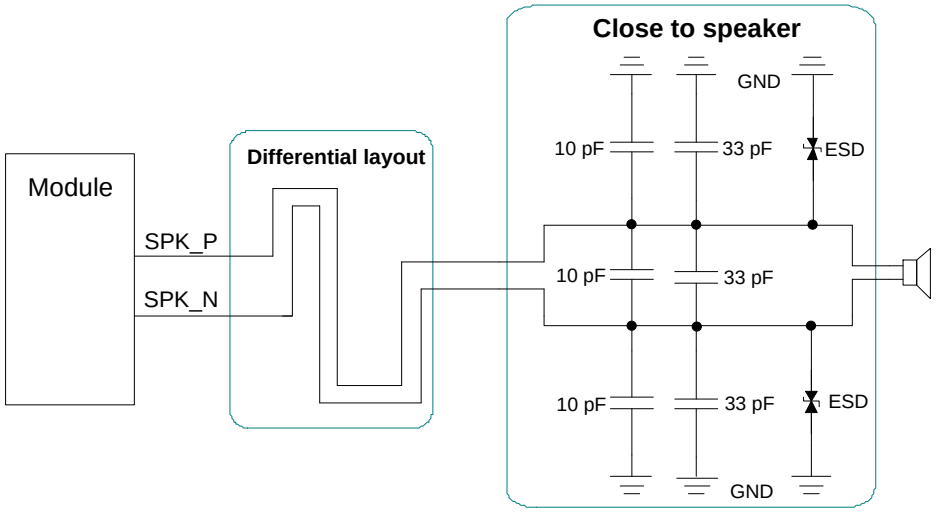


Figure 23: Handset Interface Design for Audio output channel

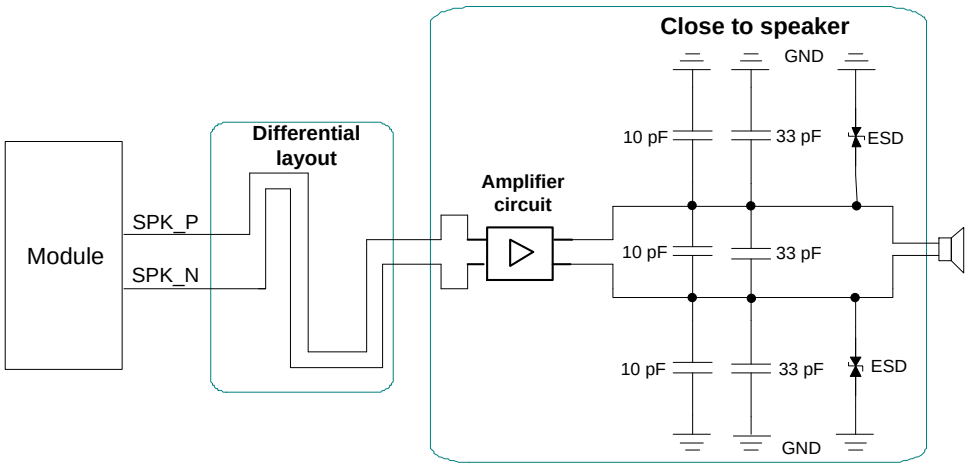


Figure 24: Speaker Interface Design with an Amplifier for Audio output channel

You can choose a suitable differential audio amplifier from the Texas Instrument's website (http://www.ti.com/). There are also other excellent audio amplifier vendors in the market.

3.12.4. Audio Characteristics

Table 16: Typical Electret Microphone Characteristics

Parameter	Min.	Typ.	Max.	Unit
Working Voltage	0	0.9	1.8	V
Working Current			90	μA
External Microphone Load Resistance		10		kΩ

Table 17: Typical Speaker Characteristics

Parameter			Min.	Typ.	Max.	Unit
Audio output	Differential	Load resistance		32		Ω
		Ref level	0		1.59	Vpp

3.13. PCM* and I2C Interfaces

The EG912Y series modules provide one Pulse Code Modulation (PCM) digital interface for audio design, and one I2C interface. The PCM interface supports the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In the primary mode, the data is sampled on the falling edge of the PCM_CLK pin and is transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256, 512 1024 or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In the auxiliary mode, the data is also sampled on the falling edge of the PCM_CLK and is transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with 256, 512, 1024 or 2048 kHz PCM_CLK at 8 kHz, 50 %-duty-cycle PCM_SYNC.

The EG912Y series modules support 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

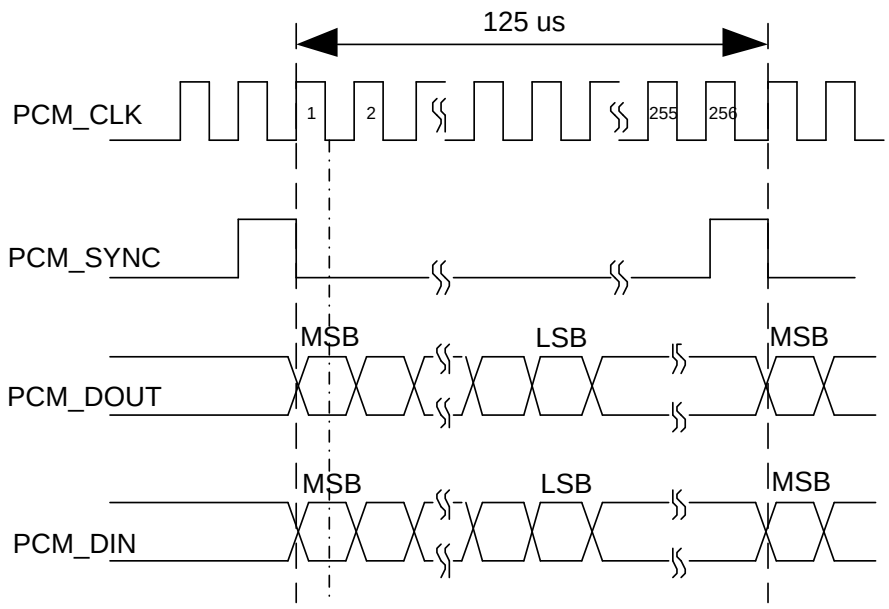


Figure 25: Primary Mode Timing

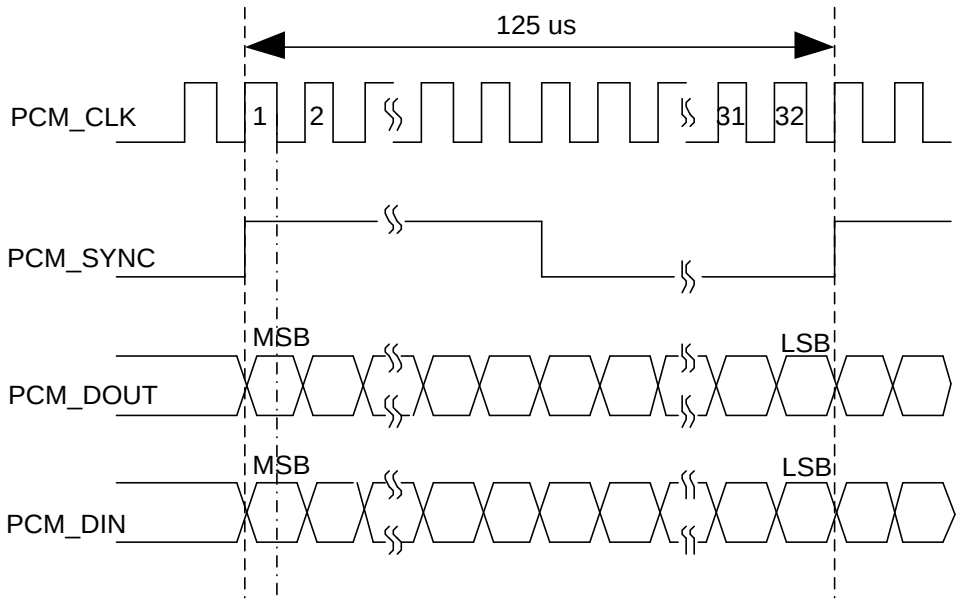


Figure 26: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 18: Pin Definition of the PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	4	DO	PCM data bit clock	1.8 V power domain
PCM_SYNC	5	IO	PCM data frame synchronization signal	1.8 V power domain
PCM_DIN	6	DI	Input PCM data	1.8 V power domain
PCM_DOUT	7	DO	Output PCM data	1.8 V power domain
I2C_SCL	40	OD	I2C serial clock	Requires an external pull-up to 1.8 V
I2C_SDA	41	OD	I2C serial data	Requires an external pull-up to 1.8 V

You can configure the clocks and modes by AT commands. The default configuration is the master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. see ***document [2]*** about **AT+QDAI** for details.

The following figure shows a reference design of PCM and I2C interfaces with the external codec.

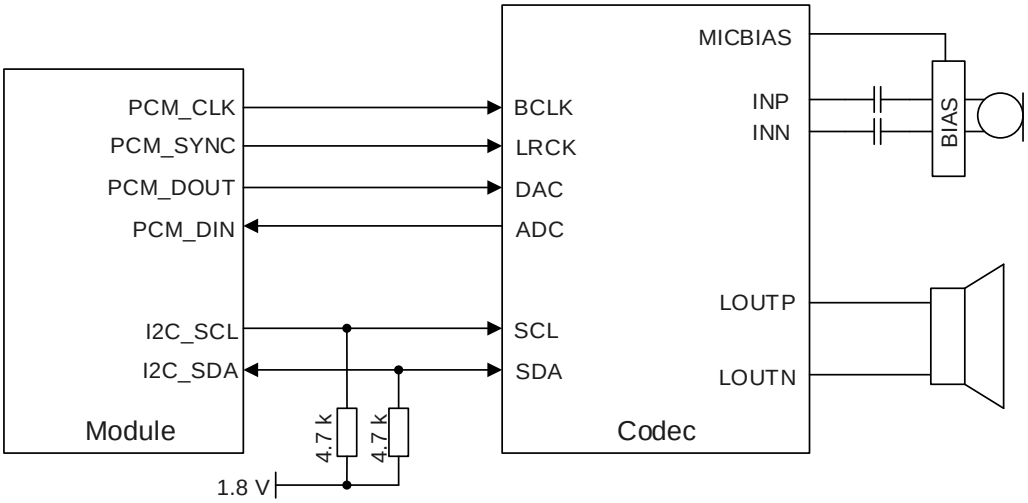


Figure 27: Reference Circuit of PCM and I2C Application with Audio Codec

NOTES

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM lines, especially for the PCM_CLK pin.
2. The EG912Y series modules work as the master device on applications pertaining to the I2C interface.
3. "*" means under development.

3.14. SPI Interface

The SPI interface of the EG912Y series modules supports master mode in which the module serves as a host. Its operation voltage is 1.8 V with clock rates up to 52 MHz.

The following table shows the pin definition of the SPI interface.

Table 19: Pin Definition of the SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CS	25	DO	Chip select signal of SPI interface	1.8 V power domain
SPI_CLK	26	DO	Clock signal of SPI interface	1.8 V power domain
SPI_MOSI	27	DO	Master output and slave input of the SPI interface	1.8 V power domain
SPI_MISO	28	DI	Master input and slave output of the SPI interface	1.8 V power domain

The following figure shows a reference design of the SPI interface with peripherals.

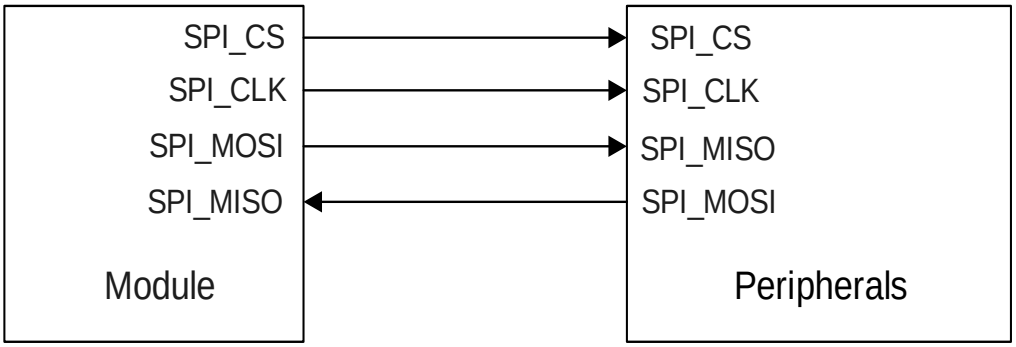


Figure 28: Reference Circuit of the SPI Interface with Peripherals

NOTE

The module provides a 1.8 V SPI interface. Add a level translator between the module and the host if your application is equipped with a 3.3 V processor or device interface.

3.15. LCM Interface

The LCM interface of the EG912Y series modules supports a maximum resolution of 240 × 320 LCD module. The interface supports 4-line serial peripheral interface (SPI) and 1 lane SPI data transmission. Additionally, it support outputting in RGB565 format.

The following table shows the pin definition of the LCM interface.

Table 20: Pin Definition of the LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_CS	16	DO	LCD CS	1.8 V power domain
LCD_TE	92	DI	LCD tearing effect	1.8 V power domain
LCD_SPI_CLK	105	DO	LCD SPI clock	1.8 V power domain
LCD_SPI_RS	106	DO	LCD Register selection	1.8 V power domain
LCD_SPI_RST	107	DO	LCD SPI Reset	1.8 V power domain
LCD_BL_K	109	OD	LCD backlight driver	Sink current drive, maximum 96 mA, adjustable
LCD_SPI_DOUT	116	DO	LCD SPI data output	1.8 V power domain

See ***document [5]*** for details about the reference design of the LCM interface.

3.16. Camera Interface

Camera interface of EG912Y series supports 1 or 2 bits SPI interface.

The following table shows the pin definition of Camera interface.

Table 21: Pin Definition of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_IOVDD	93	PO	Camera IO power	Vnorm = 1.8 V
CAM_VDD	94	PO	Camera power	Vnorm = 2.8 V
CAM_MCLK	95	DO	Camera clock	1.8 V power domain
CAM_SPI_CLK	96	DI	Camera SPI clock	1.8 V power domain
CAM_SPI_DATA0	97	DI	Camera SPI inputs 0 data bit	1.8 V power domain
CAM_SPI_DATA1	98	DI	Camera SPI inputs 1 data bit	1.8 V power domain
CAM_I2C_SCL	103	OD	Camera I2C clock	1.8 V power domain
CAM_I2C_SDA	114	OD	Camera I2C data	1.8 V power domain
MCAM_PWDN	115	DO	Camera off	1.8 V power domain
FLASH_LED	117	OD	Drives Flash/Flashlight output	Sink current drive, adjustable within the maximum 64 mA

See ***document [5]*** for details about the reference design of the Camera interface.

3.17. WLAN Interface*

The EG912Y series modules provide a SDIO 3.0 WLAN interface.

The following table shows the pin definition of the WLAN interface.

Table 22: Pin Definition of the WLAN Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SDIO_DATA0	11	IO	WLAN SDIO data bus D0	1.8 V power domain

WLAN_SDIO_DATA1	12	IO	WLAN SDIO data bus D1	1.8 V power domain
WLAN_SDIO_DATA2	13	IO	WLAN SDIO data bus D2	1.8 V power domain
WLAN_SDIO_DATA3	14	IO	WLAN SDIO data bus D3	1.8 V power domain
WLAN_EN	64	DO	Enables WLAN controlling	1.8 V power domain
WLAN_SDIO_CLK	65	DO	WLAN SDIO bus clock	1.8 V power domain
WLAN_SDIO_CMD	66	DO	WLAN SDIO bus command	1.8 V power domain
WLAN_WAKE	88	DI	Wake up the host (EG912Y series modules) via an external Wi-Fi module	1.8 V power domain

The SDIO interface rate is very high. To ensure that the interface design conforms to the SDIO 3.0 specification, follow the principles below:

- The SDIO signal cable needs to be grounded three-dimensionally, and the impedance must be controlled within 50 Ω ±10 %.
- SDIO signal lines need to be away from sensitive signals such as radio frequency, analog signals, and clock, DC-DC and other noise signals.
- The traces of WLAN_SDIO_CLK, WLAN_SDIO_DATA [0:3] and WLAN_SDIO_CMD need to be processed with equal length (the difference is less than 1 mm), and the total length of a trace must be less than 50 mm.
- The distance between SDIO signals and other signals needs to be greater than 2 times of the line width, and the bus load must be less than 15 pF.

NOTE

"*" means under development.

3.18. Network Status Indication

The module provides one network indication pin, namely NET_STATUS. The pin is used to drive a network status indication LED.

The following tables describe the pin definition and logic level changes of the NET_STATUS pin in different network status.

Table 23: Pin Definition of the Network Status Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_ STATUS	21	DO	Indicates the module's network activity status	1.8 V power domain

Table 24: Working State of the Network Status Indicator

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

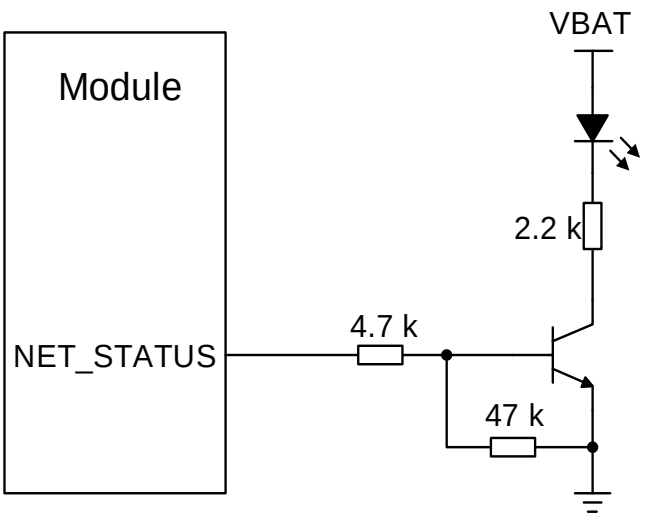


Figure 29: Reference Circuit of the Network Status Indicator

3.19. STATUS

The STATUS pin serves as the module's operation status indicator. It outputs high level voltage when the module is powered on. The following table describes the definition of the STATUS pin.

Table 25: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicates the module's operation status	1.8 V power domain. If unused, keep it open.

The following figure shows the reference circuit of STATUS.

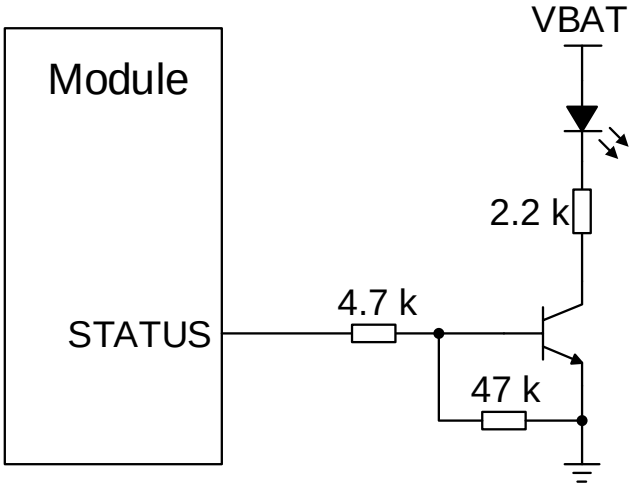


Figure 30: Reference Circuit of STATUS

NOTE

Pin STATUS cannot be pulled up before startup.

3.20. ADC Interface

The module provides two analog-to-digital converter (ADC) interfaces. You can use **AT+QADC=0** command to read the voltage value on the ADC pin. For more details about the command, see ***document [2]***.

To improve the accuracy of ADC voltage values, the traces of ADC should be surrounded by ground.

Table 26: Pin Definition of the ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose analog-to-digital converter	If unused, keep this pin open.
ADC1	2	AI	General-purpose analog-to-digital converter	If unused, keep this pin open.

The following table describes the characteristics of ADC interface.

Table 27: Characteristics of the ADC Interface

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0		VBAT_BB	V
ADC1 Voltage Range	0		VBAT_BB	V
ADC Resolution			12	Bits

NOTES

1. Do NOT supply any voltage to ADC pins when ADC pins are not powered by VBAT.
2. If the voltage from acquired from the ADC interface is greater than VABT_BB, use a resistor divider circuit for ADC application.

3.21. Behaviors of MAIN_RI

You can use **AT+QCFG="risignaltype","physical"** command to configure MAIN_RI behaviors. The default MAIN_RI behaviors can be changed by **AT+QCFG="urc/ri/ring"** command. See ***document [2]*** for details.

No matter on which port a URC is presented, the URC triggers the behavior of the MAIN_RI pin.

NOTE

You can configure one of UART port, USB AT port or USB modem port as the URC outputting port via the **AT+QURCCFG** command. The default port is USB AT port. See ***document [2]*** for details.

The default behaviors of the MAIN_RI are shown as below.

Table 28: Default Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps at high voltage level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

3.22. USB_BOOT Interface

The EG912Y series modules provide a USB_BOOT pin. Pull up USB_BOOT to 1.8 V before VDD_EXT is powered up so that the module enters emergency download mode when it is started. In this mode, the module supports software upgrade over USB interface. Restart the module to exit it from the emergency download mode.

Table 29: Pin Definition of the USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Forces the module to enter the emergency download mode	1.8 V power domain. Active high. It is recommended to reserve test point.

The following figures show the reference circuit of the USB_BOOT interface and the timing sequence of entering the emergency download mode.

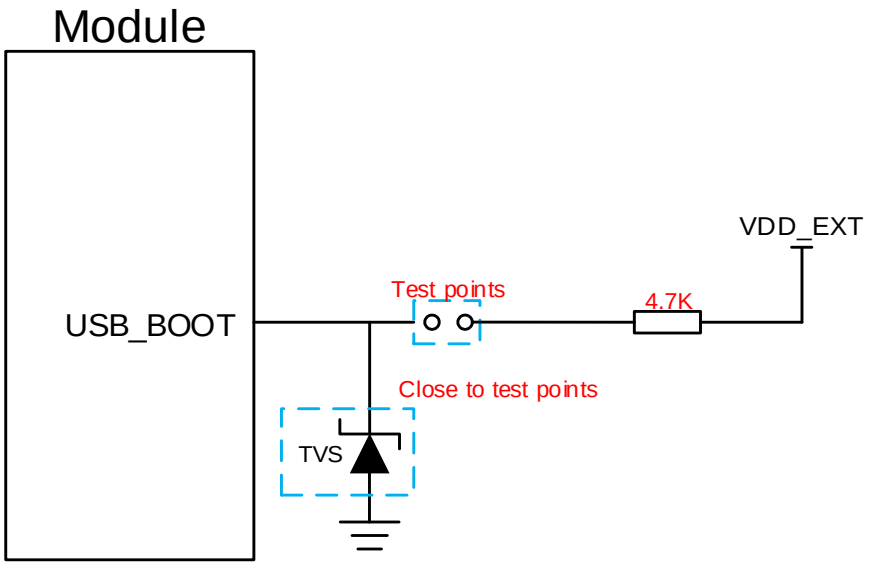


Figure 31: Reference Circuit of the USB_BOOT Interface

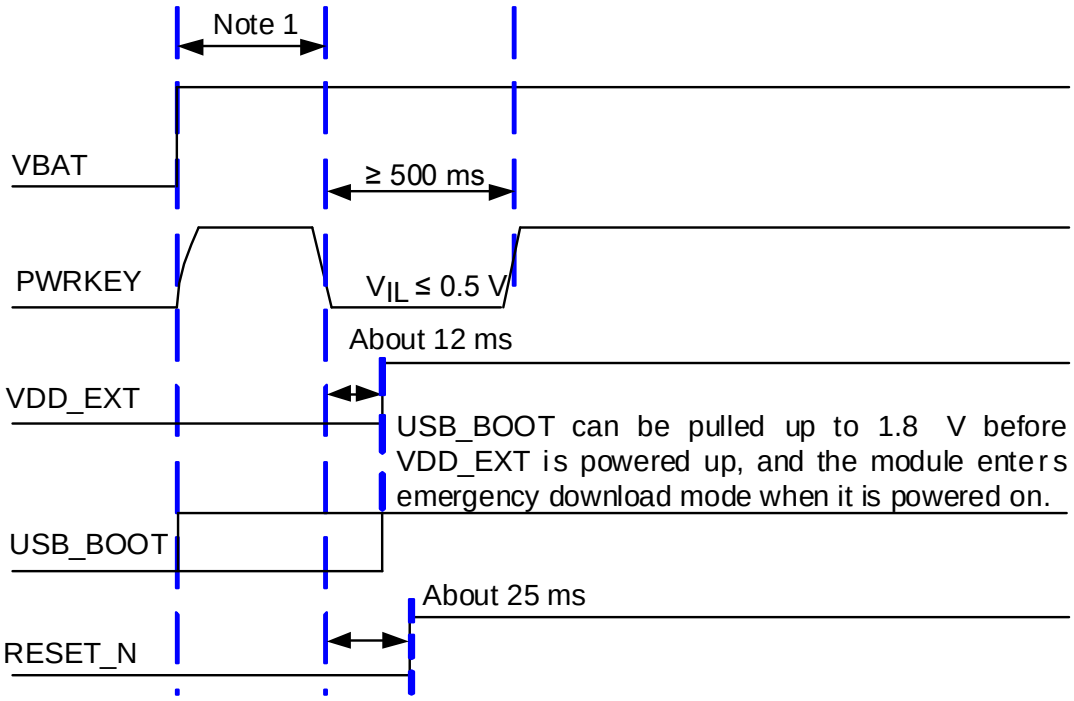


Figure 32: Timing Sequence for Entering the Emergency Download Mode

NOTES

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down the PWRKEY pin is no less than 30 ms.
2. When using MCU to control the module to enter the emergency download mode, follow the above timing sequence. Do not pull up USB_BOOT to 1.8 V before powering up VBAT. Linking the test points of USB_BOOT to 1.8 V as shown in ***Figure 31*** can manually force the module to enter the download mode.
3. Do NOT pull up USB_BOOT before startup.

4 Antenna Interface

The EG912Y series modules have a main antenna interface. The impedance of the antenna port is 50 Ω.

4.1. Main Antenna Interface

4.1.1. Pin Definition

The pin definition of the main antenna interface is shown below.

Table 30: Pin Definition of RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	IO	Main antenna	50 Ω impedance

4.1.2. Operating Frequency

Table 31: EG912Y-CN Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz

LTE-FDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2535–2675	2535–2675	MHz

Table 32: EG912Y-EU Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
GSM850	824–849	869–894	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

4.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN antenna pads is shown below. For better RF performance, reserve a π-type matching circuit. The capacitors are not mounted by default.

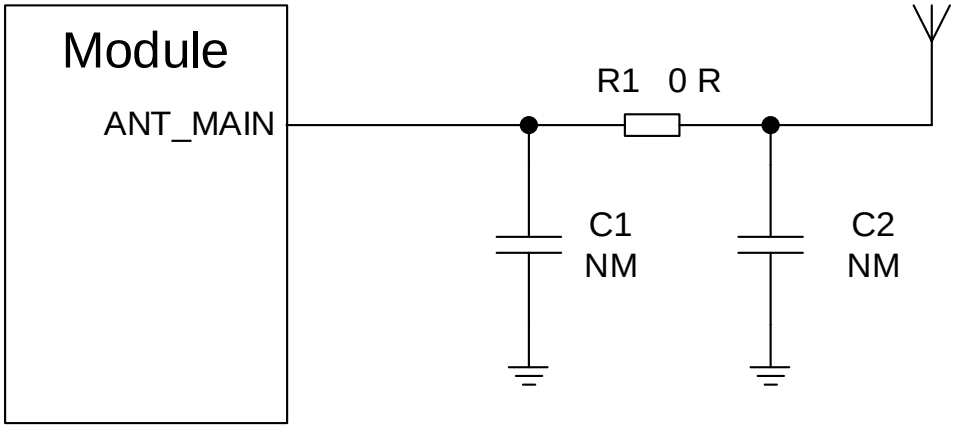


Figure 33: Reference Circuit of the RF Antenna Interface

NOTE

Place the π-type matching components (R1/C1/C2) to the antenna as close as possible.

4.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between the RF trace and the ground (S). Microstrip and coplanar waveguide are typically used in RF layout to control characteristic impedance. The following figures are reference designs of microstrip or coplanar waveguide with different PCB structures.

- The entire structure of microstrip line

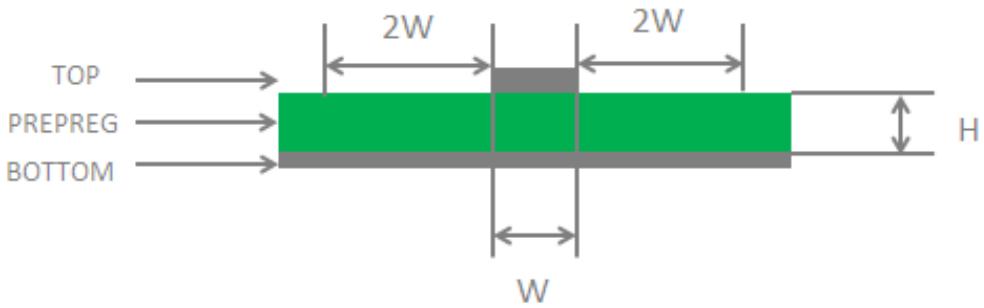


Figure 34: Microstrip Line Design on a 2-layer PCB

- The entire structure of coplanar waveguide

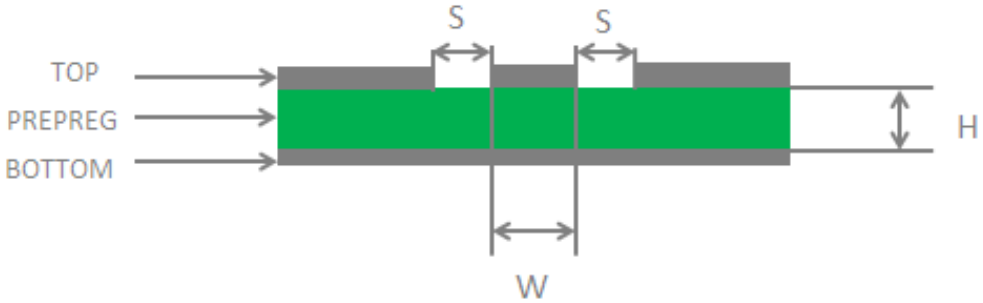


Figure 35: Coplanar Waveguide Design on a 2-layer PCB

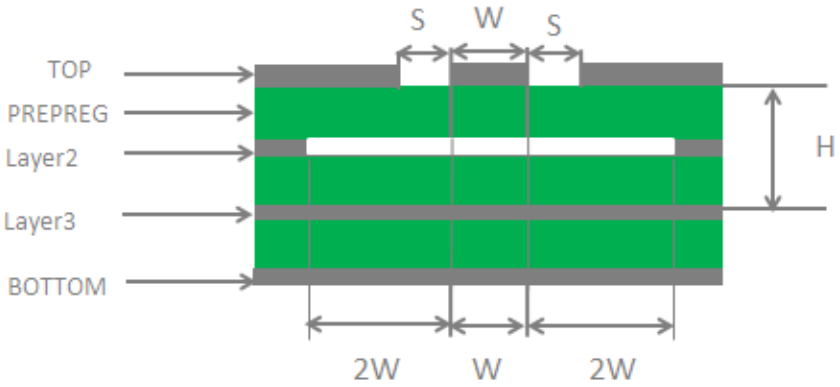


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

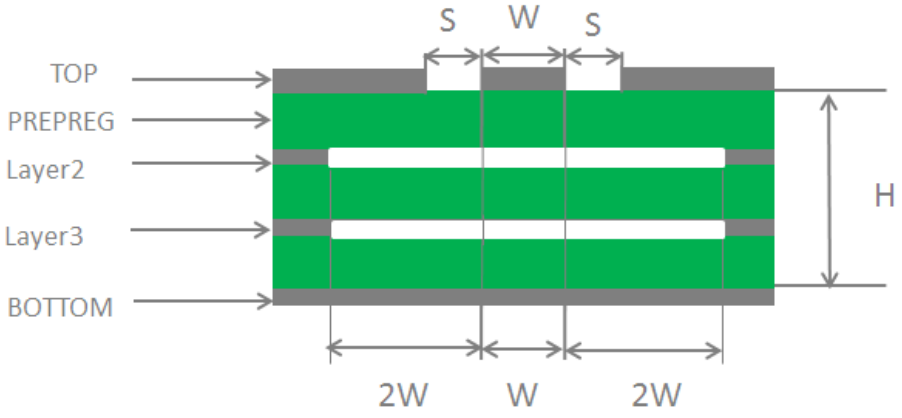


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, please refer to ***document [3]***.

4.2. Antenna Installation

4.2.1. Antenna Requirement

The following tables show the requirements on main antennas of the two variants of the EG912Yseries modules: EG912Y-CN and EG912Y-EU.

Table 33: EG912Y-CN Antenna Requirements

Type	Requirements
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: < 1 dB (EGSM900, LTE-FDD B5/B8) Cable insertion loss: < 1.5 dB (DCS1800, LTE-FDD B1/B3, LTE-TDD B34/B39) Cable insertion loss: < 2 dB (LTE-TDD B38/B40/B41)

Table 34: EG912Y-EU Antenna Requirements

Type	Requirements
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: < 1 dB (EGSM900, GSM850, LTE-FDD B5/B8/B20/B28) Cable insertion loss: < 1.5 dB (DCS1800, PCS1900, LTE-FDD B1/B3) Cable insertion loss: < 2 dB (LTE-FDD B7, LTE-TDD B38/B40/B41)

4.2.2. Recommended RF Connector for Antenna Installation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by *Hirose*.

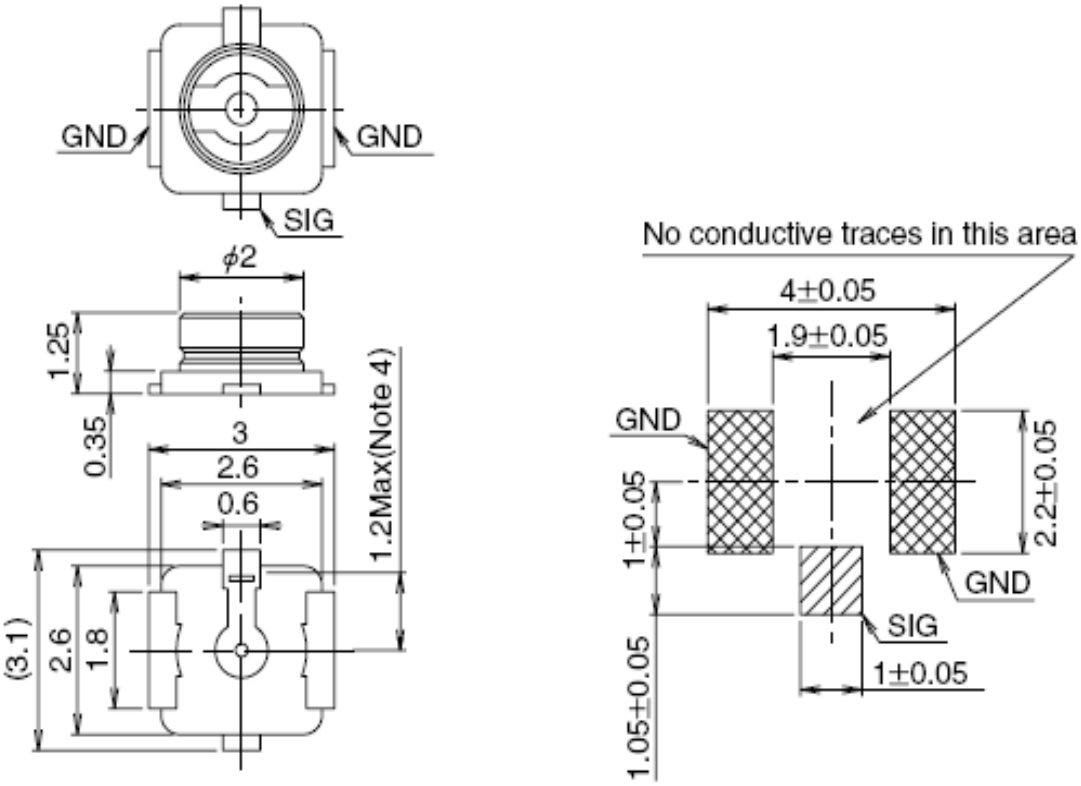


Figure 38: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

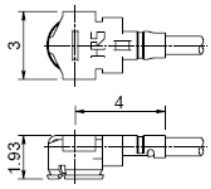
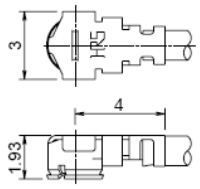
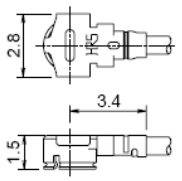
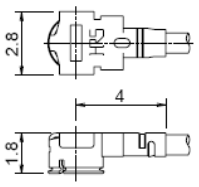
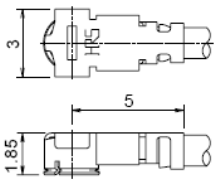
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 39: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of the mated connector.

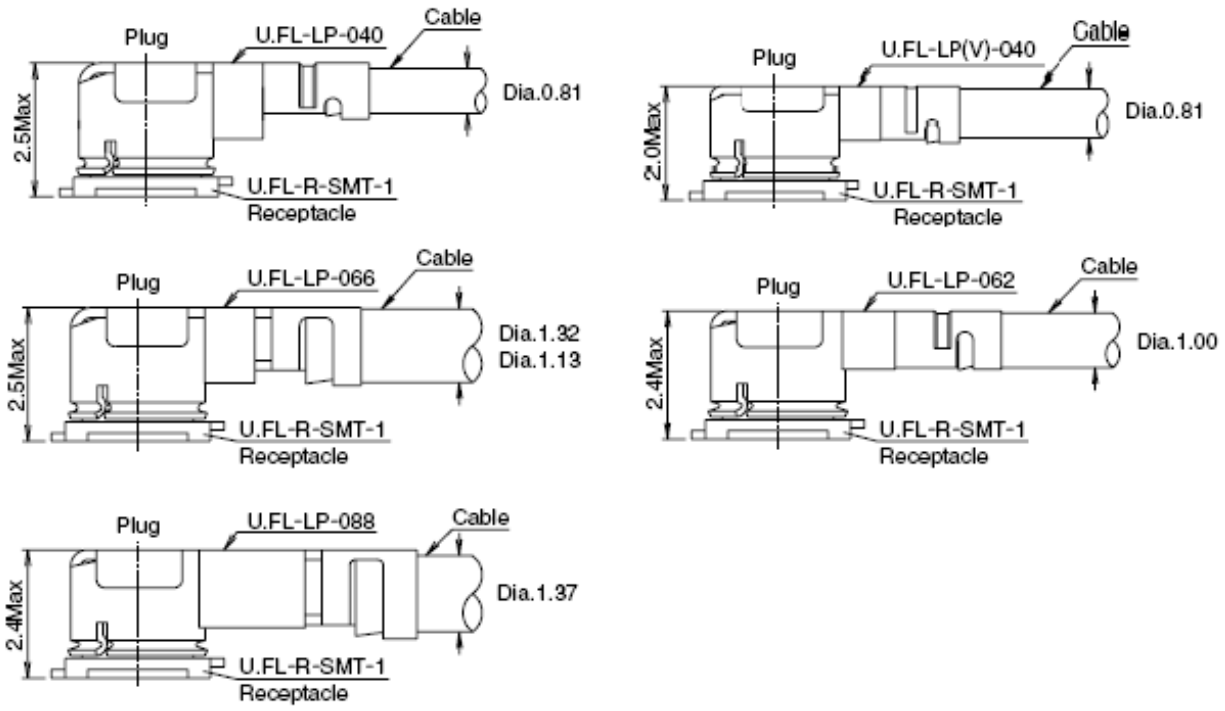


Figure 40: Space Factor of the Mated Connector (Unit: mm)

For more details, visit http://www.hirose.com.

5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

The absolute maximum ratings for power supply and voltage on digital and analog pins of the modules are listed in the following table.

Table 35: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB	-0.3	6	V
VBAT_RF	-0.3	6	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V

5.2. Power Supply Ratings

Table 36: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.4	3.8	4.5	V

	Voltage drop during burst transmission	Maximum power control level on EGSM900/GSM850/PCS1900			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900/GSM850/PCS1900		1.8	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

5.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 37: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within the operating temperature range, the module meets 3GPP specifications..
2. [2)] Within extended temperature range, the module maintain functions such as voice, SMS, data transmission, emergency call*, etc., without any unrecoverable malfunction. Radio spectrum and radio network will not be influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module meets 3GPP specifications again.
3. "*" means under development.

5.4. Current Consumption

The values of current consumption are shown below.

Table 38: EG912Y-CN Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	15	μA
	Sleep state	**AT+CFUN=0** (USB disconnected)	0.75	mA
		AT+CFUN=4 (USB disconnected)	0.8	mA
		EGSM900 @ DRX = 2 (USB disconnected)	1.5	mA
		EGSM900 @ DRX = 5 (USB disconnected)	1.1	mA
		EGSM900 @ DRX = 9 (USB disconnected)	1	mA
		DCS1800 @ DRX = 2 (USB disconnected)	1.5	mA
		DCS1800 @ DRX = 5 (USB disconnected)	1.1	mA
		DCS1800 @ DRX = 9 (USB disconnected)	1	mA
		LTE-FDD @ PF = 32 (USB disconnected)	1.8	mA
		LTE-FDD @ PF = 64 (USB disconnected)	1.3	mA
		LTE-FDD @ PF = 128 (USB disconnected)	1.1	mA
		LTE-FDD @ PF = 256 (USB disconnected)	0.9	mA
		LTE-TDD @ PF = 32 (USB disconnected)	1.8	mA
		LTE-TDD @ PF = 64 (USB disconnected)	1.3	mA
		LTE-TDD @ PF = 128 (USB disconnected)	1.1	mA
		LTE-TDD @ PF = 256 (USB disconnected)	0.9	mA
	Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.5	mA
		EGSM900 @ DRX = 5 (USB connected)	21.5	mA
		LTE-FDD @ PF = 64 (USB disconnected)	12.5	mA

		LTE-FDD @ PF = 64 (USB connected)	21	mA
		LTE-TDD @ PF = 64 (USB disconnected)	12.5	mA
		LTE-TDD @ PF = 64 (USB connected)	21	mA
	GPRS data transfer	EGSM900 4DL/1UL @ 32.35 dBm	TBD	mA
		EGSM900 3DL/2UL @ 32.16 dBm	TBD	mA
		EGSM900 2DL/3UL @ 30.57 dBm	TBD	mA
		EGSM900 1DL/4UL @ 29.45 dBm	TBD	mA
		DCS1800 4DL/1UL @ 29.14 dBm	TBD	mA
		DCS1800 3DL/2UL @ 29.07 dBm	TBD	mA
		DCS1800 2DL/3UL @ 28.97 dBm	TBD	mA
		DCS1800 1DL/4UL @ 28.88 dBm	TBD	mA
	EDGE data transfer	EGSM900 4DL/1UL PCL = 8 @ 26.88 dBm	TBD	mA
		EGSM900 3DL/2UL PCL = 8 @ 26.84 dBm	TBD	mA
		EGSM900 2DL/3UL PCL = 8 @ 26.76 dBm	TBD	mA
		EGSM900 1DL/4UL PCL = 8 @ 26.54 dBm	TBD	mA
		DCS1800 4DL/1UL PCL = 2 @ 25.66 dBm	TBD	mA
		DCS1800 3DL/2UL PCL = 2 @ 25.59 dBm	TBD	mA
		DCS1800 2DL/3UL PCL = 2 @ 25.51dBm	TBD	mA
		DCS1800 1DL/4UL PCL = 2 @ 25.38 dBm	TBD	mA
	LTE data transfer	LTE-FDD B1 @ 23.37 dBm	TBD	mA
		LTE-FDD B3 @ 22.97 dBm	TBD	mA
		LTE-FDD B7 @ 23.17 dBm	TBD	mA
		LTE-FDD B8 @ 23.04 dBm	TBD	mA
		LTE-FDD B20 @ 23.21 dBm	TBD	mA
		LTE-FDD B28A @ 22.76 dBm	TBD	mA

	GSM voice call	EGSM900 PCL = 5 @ 32.36 dBm	TBD	mA
		DCS1800 PCL = 0 @ 29.19 dBm	TBD	mA

Table 39: EG912Y-EU Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	15	μA
	Sleep state	**AT+CFUN=0** (USB disconnected)	0.75	mA
		AT+CFUN=4 (USB disconnected)	0.8	mA
		GSM850 @ DRX = 2 (USB disconnected)	TBD	mA
		GSM850 @ DRX = 5 (USB disconnected)	TBD	mA
		GSM850 @ DRX = 9 (USB disconnected)	TBD	mA
		EGSM900 @ DRX = 2 (USB disconnected)	1.5	mA
		EGSM900 @ DRX = 5 (USB suspended)	1.1	mA
		EGSM900 @ DRX = 9 (USB disconnected)	1	mA
		DCS1800 @ DRX = 2 (USB disconnected)	1.5	mA
		DCS1800 @ DRX = 5 (USB disconnected)	1.1	mA
		DCS1800 @ DRX = 9 (USB disconnected)	1	mA
		PCS1900 @ DRX = 2 (USB disconnected)	TBD	mA
		PCS1900 @ DRX = 5 (USB disconnected)	TBD	mA
		PCS1900 @ DRX = 9 (USB disconnected)	TBD	mA
		LTE-FDD @ PF = 32 (USB disconnected)	1.8	mA
		LTE-FDD @ PF = 64 (USB disconnected)	1.3	mA
		LTE-FDD @ PF = 128 (USB disconnected)	1.1	mA
		LTE-FDD @ PF = 256 (USB disconnected)	0.9	mA
		LTE-TDD @ PF = 32 (USB disconnected)	1.8	mA

	LTE-TDD @ PF = 64 (USB disconnected)	1.3	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.1	mA
	LTE-TDD @ PF = 256 (USB disconnected)	0.9	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.5	mA
	EGSM900 @ DRX = 5 (USB connected)	21.5	mA
	LTE-FDD @ PF = 64 (USB disconnected)	12.5	mA
	LTE-FDD @ PF = 64 (USB connected)	21	mA
	LTE-TDD @ PF = 64 (USB disconnected)	12.5	mA
	LTE-TDD @ PF = 64 (USB connected)	21	mA
GPRS data transfer	EGSM900 4DL/1UL @ 32.35 dBm	TBD	mA
	EGSM900 3DL/2UL @ 32.16 dBm	TBD	mA
	EGSM900 2DL/3UL @ 30.57 dBm	TBD	mA
	EGSM900 1DL/4UL @ 29.45 dBm	TBD	mA
	DCS1800 4DL/1UL @ 29.14 dBm	TBD	mA
	DCS1800 3DL/2UL @ 29.07 dBm	TBD	mA
	DCS1800 2DL/3UL @ 28.97 dBm	TBD	mA
	DCS1800 1DL/4UL @ 28.88 dBm	TBD	mA
EDGE data transfer	EGSM900 4DL/1UL PCL = 8 @ 26.88 dBm	TBD	mA
	EGSM900 3DL/2UL PCL = 8 @ 26.84 dBm	TBD	mA
	EGSM900 2DL/3UL PCL = 8 @ 26.76 dBm	TBD	mA
	EGSM900 1DL/4UL PCL = 8 @ 26.54 dBm	TBD	mA
	DCS1800 4DL/1UL PCL = 2 @ 25.66 dBm	TBD	mA
	DCS1800 3DL/2UL PCL = 2 @ 25.59 dBm	TBD	mA
	DCS1800 2DL/3UL PCL = 2 @ 25.51dBm	TBD	mA
	DCS1800 1DL/4UL PCL = 2 @ 25.38 dBm	TBD	mA

	LTE data transfer	LTE-FDD B1 @ 23.37 dBm	TBD	mA
		LTE-FDD B3 @ 22.97 dBm	TBD	mA
		LTE-FDD B7 @ 23.17 dBm	TBD	mA
		LTE-FDD B8 @ 23.04 dBm	TBD	mA
		LTE-FDD B20 @ 23.21 dBm	TBD	mA
		LTE-FDD B28A @ 22.76 dBm	TBD	mA
	GSM voice call	EGSM900 PCL = 5 @ 32.36 dBm	TBD	mA
		DCS1800 PCL = 0 @ 29.19 dBm	TBD	mA

5.5. RF Output Power

The following table shows the RF output power of the EG912Y series modules.

Table 40: EG912Y-CN RF Output Power

Frequency	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 41: EG912Y-EU RF Output Power

Frequency	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
GSM850	33 dBm ±2 dB	5 dBm ±5 dB

DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
GSM850 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/ B8/B20/B28	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 4.0 dB. The design conforms to the GSM specifications as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

5.6. RF Receiving Sensitivity

The following tables show the conducted RF receiving sensitivity of the EG912Y series modules.

Table 42: EG912Y-CN Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP
EGSM900	-109 dBm	NA	NA	-102 dBm
DCS1800	-107.5 dBm	NA	NA	-102 dBm
LTE-FDD B1 (10 MHz)	-97.5 dBm	NA	NA	-96.3 dBm
LTE-FDD B3 (10 MHz)	-97.5 dBm	NA	NA	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99 dBm	NA	NA	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.5 dBm	NA	NA	-93.3 dBm
LTE-TDD B34 (10 MHz)	-98 dBm	NA	NA	-96.3 dBm

LTE-TDD B38 (10 MHz)	-97.5 dBm	NA	NA	-96.8 dBm
LTE-TDD B39 (10 MHz)	-98 dBm	NA	NA	-96.3 dBm
LTE-TDD B40 (10 MHz)	-97.5 dBm	NA	NA	-96.3 dBm
LTE-TDD B41 (10 MHz)	-97.5 dBm	NA	NA	-94.3 dBm

Table 43: EG912Y-EU Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP
EGSM900	-108.5 dBm	NA	NA	-102 dBm
DCS1800	-108.5 dBm	NA	NA	-102 dBm
GSM850	-108 dBm	NA	NA	-102 dBm
PCS1900	-108 dBm	NA	NA	-102 dBm
LTE-FDD B1 (10 MHz)	-97.5 dBm	NA	NA	-96.3 dBm
LTE-FDD B3 (10 MHz)	-97.5 dBm	NA	NA	-93.3 dBm
LTE-FDD B5 (10 MHz)	-98.5 dBm	NA	NA	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.5 dBm	NA	NA	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.5 dBm	NA	NA	-93.3 dBm
LTE-FDD B20 (10 MHz)	-98 dBm	NA	NA	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98 dBm	NA	NA	-94.8 dBm
LTE-TDD B38 (10 MHz)	-97.5 dBm	NA	NA	-96.3 dBm
LTE-TDD B40 (10 MHz)	-97.5 dBm	NA	NA	-96.3 dBm
LTE-TDD B41 (10 MHz)	-97.5 dBm	NA	NA	-93.3 dBm

5.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any

application that incorporates the module.

The following table shows the EG912Y series modules' electrostatic discharge characteristics.

Table 44: Electrostatic Discharge Characteristics (25 ºC, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	TBD	TBD	kV
Antenna Interface	TBD	TBD	kV
Other Interfaces	TBD	TBD	kV

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

6.1. Mechanical Dimensions of the Module

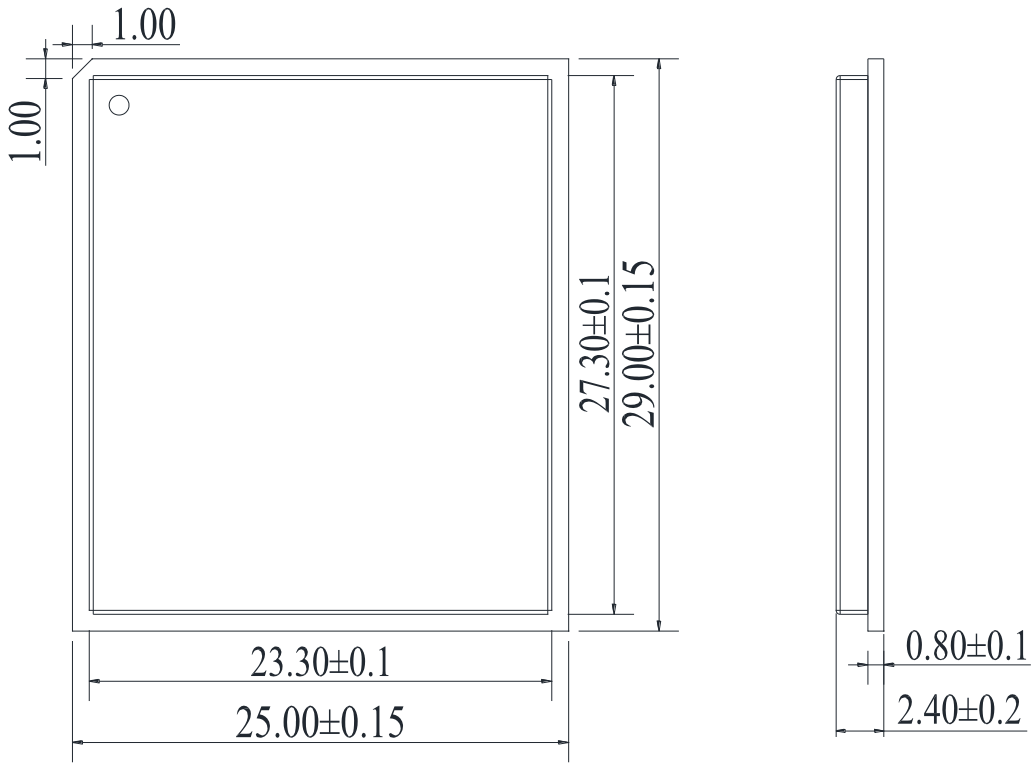


Figure 41: Module Dimensions (Top view and side view)

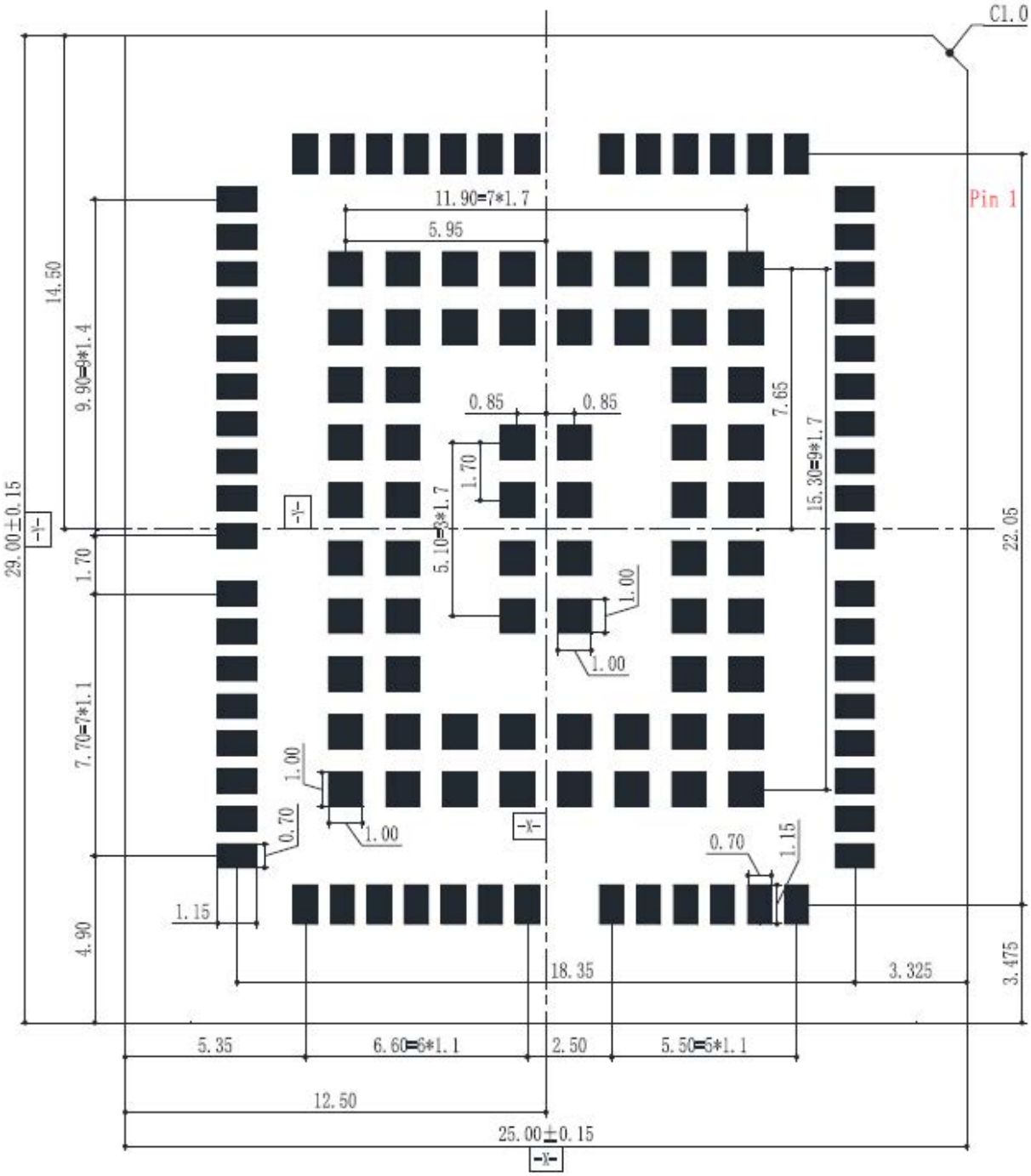


Figure 42: Module Dimensions (Bottom view)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

6.2. Recommended Footprint

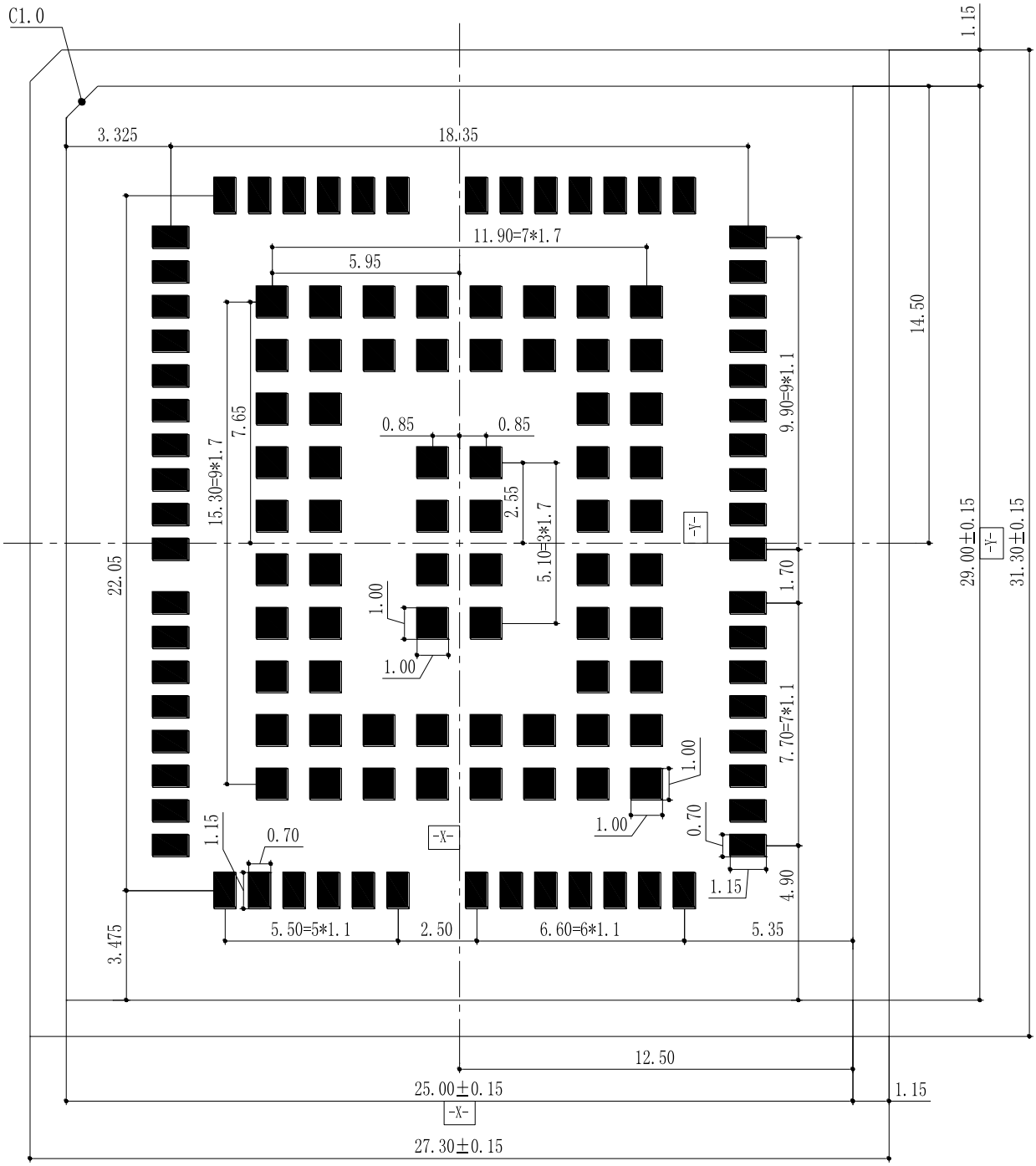


Figure 43: Recommended Footprint (Top View)

NOTE

For easy maintenance of this module, it is recommended to keep no less than 3 mm between the module and other components on a motherboard.

6.3. Top and Bottom Views of the Module

Figure 44: Top View of the Module

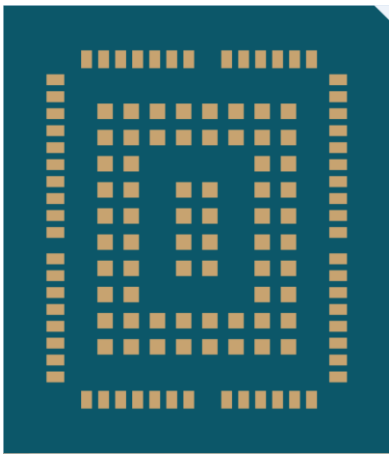


Figure 45: Bottom View of the Module

NOTE

These are renderings of the EG912Y series modules. For authentic appearance, see the modules received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

The EG912Y series modules are provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.
2. Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, please refer to *IPC/JEDEC J-STD-033* for baking procedure.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 238–246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

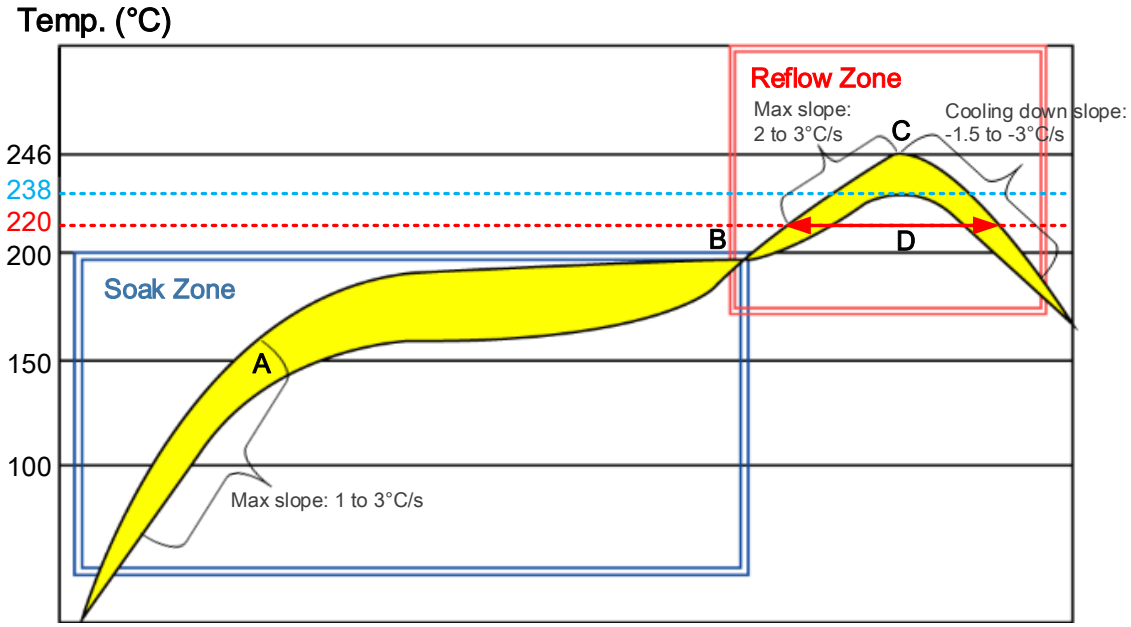


Figure 46: Recommended Reflow Soldering Thermal Profile

Table 45: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 220 °C)	45–70 s
Max temperature	238–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.

7.3. Packaging

The EG912Y series modules are delivered in carrier tape and reel packages. Each reel contains 250 modules. The figure below shows the package details, measured in the unit of millimeter (mm).

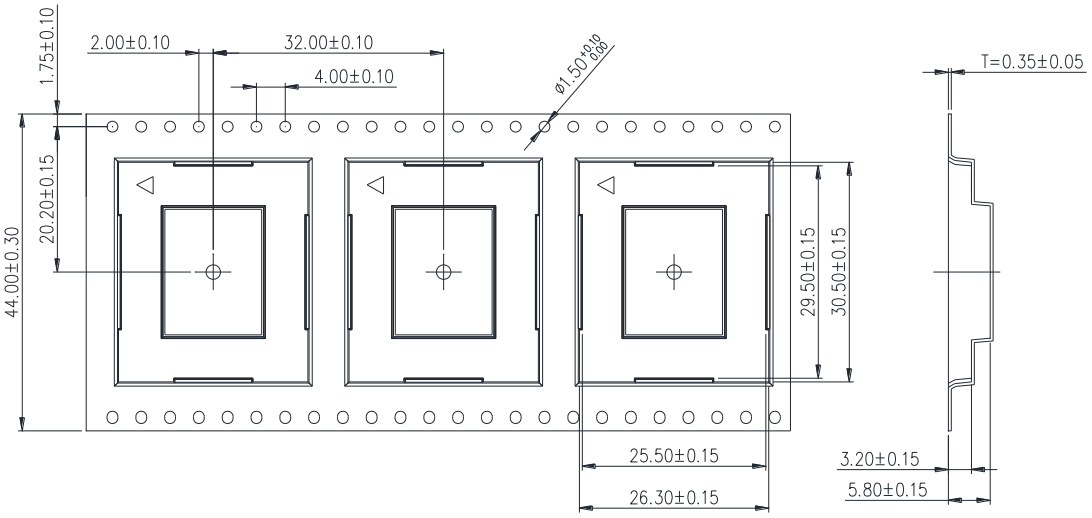


Figure 47: Carrier Tape Dimensions

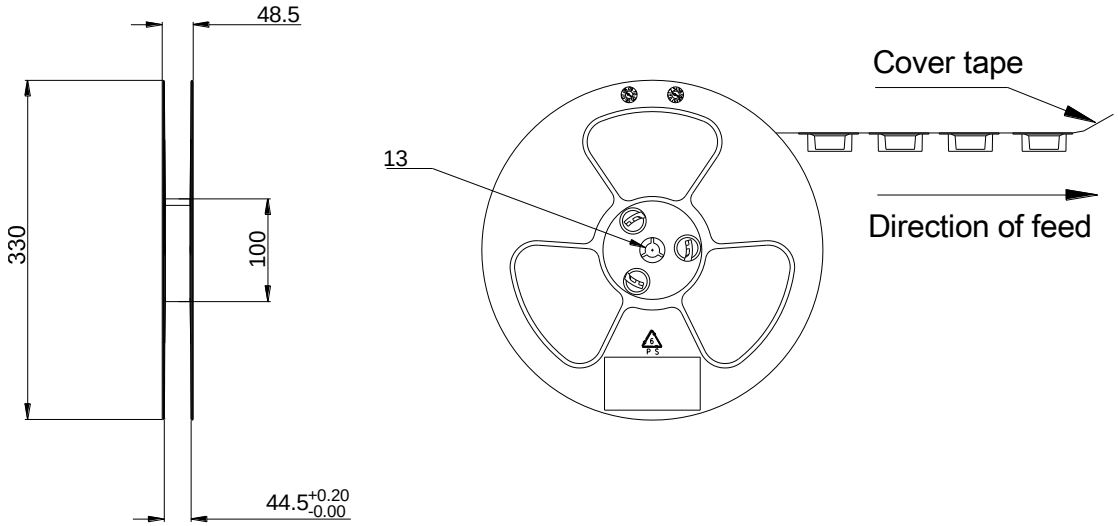


Figure 48: Reel Dimensions

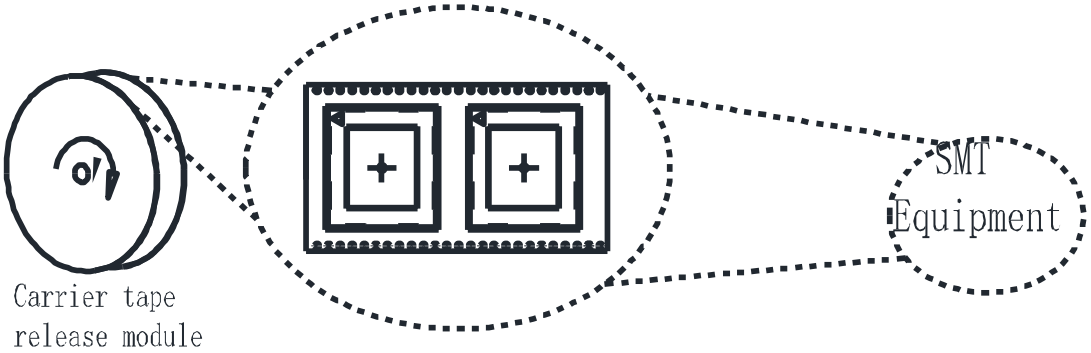


Figure 49: Tape Rolling-up Directions

8 Appendix A References

Table 46: Related Documents

SN	Document Name	Remark
[1]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide
[2]	Quectel_EC200x&EG912Y&EC100Y_Series_AT_Commands_Manual	AT commands manual for EC100Y-CN, EG912Y Series, EC200T and EC200S
[3]	Quectel_RF_Layout_Application_Note	RF layout application note
[4]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB user guide for UMTS&LTE modules
[5]	Quectel_EG912Y_Series_Reference_Design	EG912Y Series Reference Design
[6]	Quectel_LTE_Module_Thermal_Design_Guide	Thermal design guide for LTE standard, LTE-A and Automotive modules

Table 47: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
bps	Bit per Second
CHAP	Challenge-Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DL	Downlink

MAIN_DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
FOTA	Firmware Over-the-Air
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
GMSK	Gaussian Filtered Minimum Shift Keying
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current Value
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station (GSM engine)

MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PF	Paging Frame
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TXD	Transmission Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value

V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value
V_{I}min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WLAN	Wireless Local Area Network

9 Appendix B GPRS Coding Schemes

Table 48: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl. USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded (Bits)	456	588	676	456
Punctured (Bits)	0	132	220	-
Data Rate (kb/s)	9.05	13.4	15.6	21.4

10 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specifications. Multi-slot classes are product-dependent, and they determine the maximum achievable data rates in both the uplink and downlink directions. The multi-slot mode is denoted as "3 + 1" or "2 + 2", and the first number represents the quantity of downlink timeslots, while the second number indicates the quantity of uplink timeslots. The active slots determine the total number of slots that the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table:

Table 49: GPRS Multi-slot Classes

Multi-slot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5

13	3	3	NA
14	4	4	NA
15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

11 Appendix D EDGE Modulation and Coding Schemes

Table 50: EDGE Modulation and Coding Schemes

Coding Schemes	Modulation	Coding Family	1 Timeslot	2 Timeslots	4 Timeslots
CS-1:	GMSK	/	9.05 kbps	18.1 kbps	36.2 kbps
CS-2:	GMSK	/	13.4 kbps	26.8 kbps	53.6 kbps
CS-3:	GMSK	/	15.6 kbps	31.2 kbps	62.4 kbps
CS-4:	GMSK	/	21.4 kbps	42.8 kbps	85.6 kbps
MCS-1	GMSK	C	8.80 kbps	17.60 kbps	35.20 kbps
MCS-2	GMSK	B	11.2 kbps	22.4 kbps	44.8 kbps
MCS-3	GMSK	A	14.8 kbps	29.6 kbps	59.2 kbps
MCS-4	GMSK	C	17.6 kbps	35.2 kbps	70.4 kbps
MCS-5	8-PSK	B	22.4 kbps	44.8 kbps	89.6 kbps
MCS-6	8-PSK	A	29.6 kbps	59.2 kbps	118.4 kbps
MCS-7	8-PSK	B	44.8 kbps	89.6 kbps	179.2 kbps
MCS-8	8-PSK	A	54.4 kbps	108.8 kbps	217.6 kbps
MCS-9	8-PSK	A	59.2 kbps	118.4 kbps	236.8 kbps