FG50V Hardware Design

Wi-Fi/BT Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2019-11-15	Jared WANG/ Felix FU	Initial

Contents

Table Index

Figure Index

1 Introduction

This document defines the FG50V module and describes its air interface and hardware interfaces which are connected with customers' applications.

The document helps customers quickly understand module interface specifications, as well as the electrical and mechanical details. Associated with application notes and user guides, customers can use FG50V module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating FG50V module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

FG50V is a Wi-Fi and Bluetooth (BT) module with low power consumption. It is a single-die WLAN (Wireless Local Area Network) and BT combo solution supporting IEEE 802.11 a/b/g/n/ac/ax 2.4G&5G WLAN standards and BT5.1 standard, which enables seamless integration of WLAN and BT Low Energy technologies.

FG50V supports a low-power PCIe Gen 2 interface for WLAN and a UART/PCM interface for BT, and also supports LTE&WLAN/BT coexistence interface. It is designed to be used in conjunction with Quectel 5G module RG500Q so as to provide RG500Q with WLAN and BT functions.

NOTE

BT function of FG50V is still under development.

2.2. Key Features

The following table describes the key features of FG50V module.

Table 1: Key Features

Features	Details
Power Supply	Core supply voltage: 0.95V, 1.35V, 1.95V I/O supply voltage: 1.8V RF supply voltage: 3.85V
Operating Frequency	● 2.4GHz WLAN: 2.412GHz~2.472GHz ● 5GHz WLAN: 5.180GHz~5.825GHz ● BT: 2.402GHz~2.480GHz
Transmission Data Rates	● 802.11b: 1Mbps, 2Mbps, 5.5Mbps, 11Mbps ● 802.11g: 6Mbps, 9Mbps, 12Mbps, 18Mbps, 24Mbps, 36Mbps, 48Mbps,

	54Mbps ● 802.11n: 6.5Mbps, 13Mbps, 19.5Mbps, 26Mbps, 39Mbps, 52Mbps, 58.5Mbps, 65Mbps ● 802.11a: 6Mbps, 9Mbps, 12Mbps, 18Mbps, 24Mbps, 36Mbps, 48Mbps, 54Mbps ● 802.11ac: VHT20 (MCS0-11), VHT40 (MCS0-11), VHT80 (MCS0-11) ● 802.11ax: HE20 (MCS0-11), HE40 (MCS0-11), HE80 (MCS0-11),
Transmitting Power	**2.4G** 802.11b/11Mbps: 19.5dBm 802.11g/54Mbps: 17dBm 802.11n/HT20 MCS7: 16dBm 802.11n/HT40 MCS7: 15.5dBm 802.11ac/VHT20 MCS8: 9dBm 802.11ac/VHT40 MCS11: 13.5dBm 802.11ac/VHT80 MCS11: 13dBm 802.11ax/HE20 MCS11: 13.5dBm 802.11ax/HE40 MCS11: 13dBm **5G** 802.11b/11Mbps: 17dBm 802.11g/54Mbps: 14.5dBm 802.11n/HT20 MCS7: 13.5dBm 802.11n/HT40 MCS7: 13dBm 802.11ac/VHT20 MCS11: 11dBm 802.11ac/VHT40 MCS11: 10.5dBm 802.11ac/VHT80 MCS11: 11dBm 802.11ax/HE20 MCS11: 11dBm 802.11ax/HE40 MCS11: 10.5dBm 802.11ax/HE80 MCS11: 10dBm
Protocol Features	● IEEE 802.11 a/b/g/n/ac/ax ● Bluetooth 5.1
Operation Mode	AP, STA
Modulation	BPSK, QPSK, CCK, 16QAM, 64QAM, 256QAM, 1024QAM
WLAN Interface	PCIe
BT Interface*	UART and PCM
Antenna Interface	● Wi-Fi/BT antenna interface ● 50Ω impedance
Physical Characteristics	● Size: (19.5±0.2)mm × (21.5±0.2)mm × (2.1±0.2)mm ● Package: LGA ● Weight: TBD
Temperature Range	● Operating temperature range: -35°C~+75°C [1)]

	● Extended temperature range : -40°C~+85°C [2)] ● Storage temperature range: -40°C~+90°C
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operation temperature range, the module is IEEE compliant.
2. [2)] Within extended temperature range, the module remains the ability for data transmission. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their values and exceed the specified tolerances. When the temperature returns to the normal operation temperature level, the module will meet IEEE specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of FG50V module.

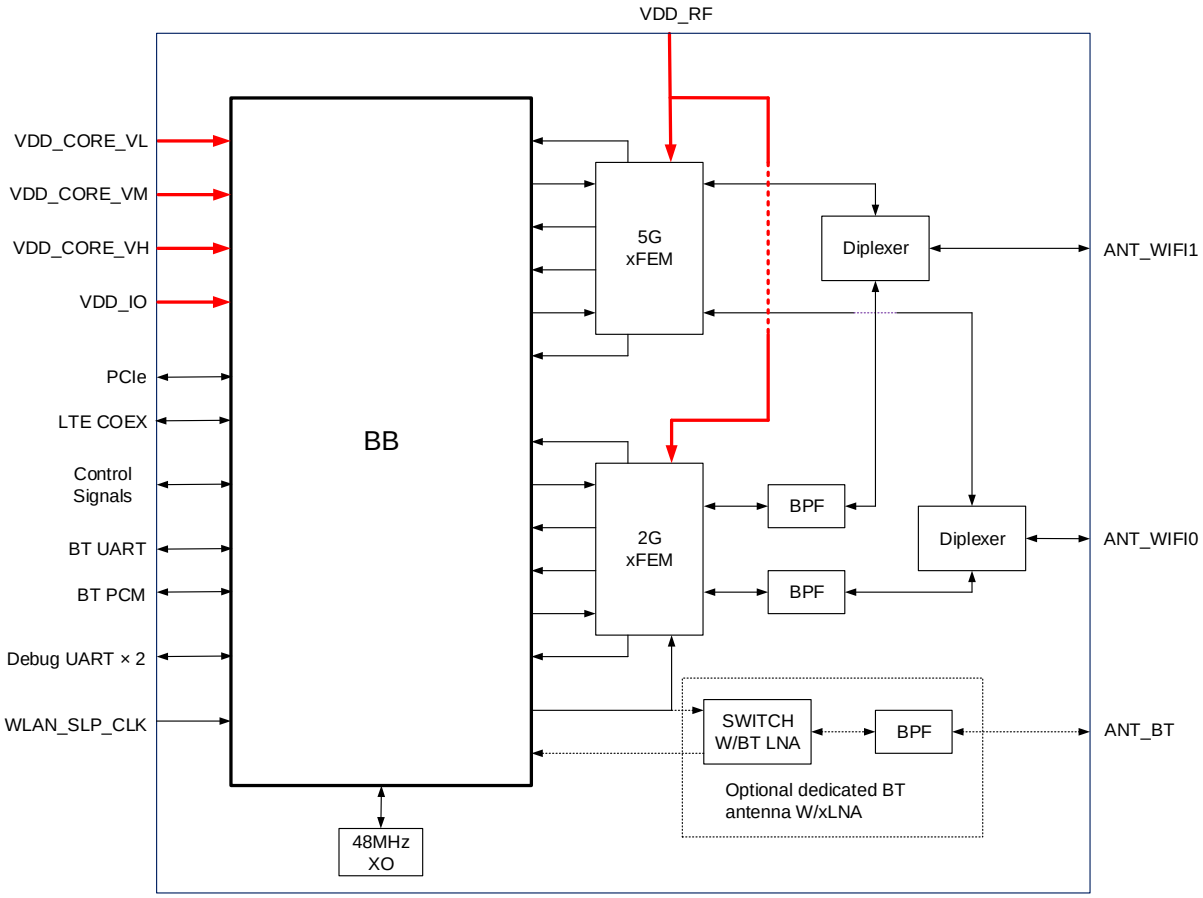


Figure 1: Functional Diagram of FG50V Module

2.4. Evaluation Board

In order to help customers develop applications with FG50V module conveniently, Quectel supplies the evaluation board (EVB), USB to RS232 converter cable, USB data cable, power adapter, antenna and other peripherals to control or test the module. For more details, please refer to ***document [1]*** and/or ***document [2]***.

3 Application Interfaces

3.1. General Description

FG50V module is equipped with 108 LGA pins that can be connected to the cellular application platform. The subsequent chapters will provide a detailed introduction to the following interfaces and pins of the module:

- Power supply
- WLAN interface
- BT interface*
- Control signal pins
- Coexistence interfaces
- WLAN_SLP_CLK interface
- RF antenna interfaces

3.2. Pin Assignment

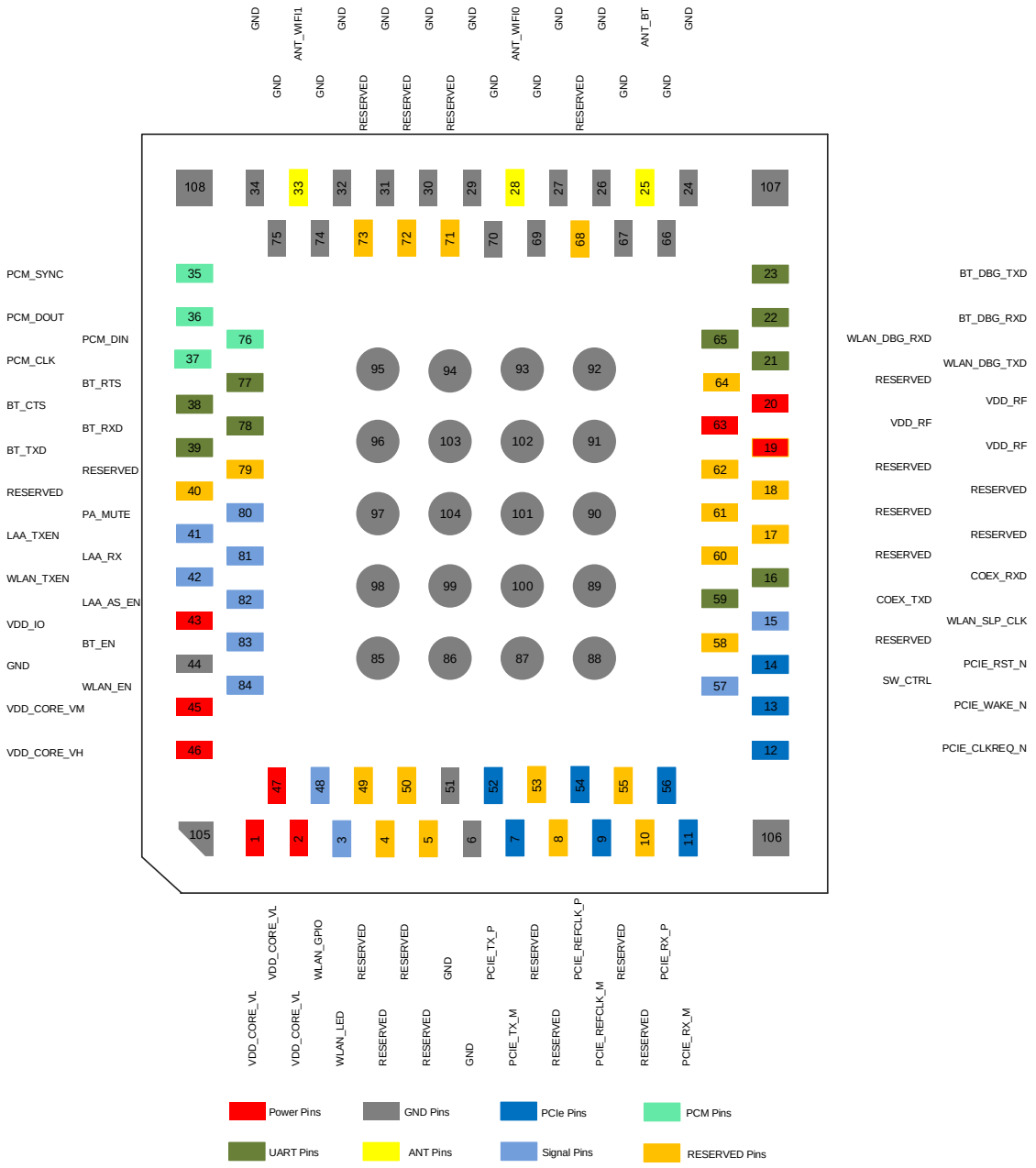


Figure 2: Pin Assignment (Top View)

NOTE

Please keep all RESERVED pins open.

3.3. Pin Description

The following tables show the pin description of FG50V module.

Table 2: I/O Parameters Definition

Type	Description
DI	Digital Input
DO	Digital Output
IO	Bidirectional
PI	Power Input

Table 3: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_CORE_VL	1, 2, 47	PI	Voltage for core, low voltage	Vmin =0.9V Vnorm =0.95V Vmax =1.0V	It must be provided with sufficient current up to 2.5A.
VDD_CORE_VM	45	PI	Voltage for core, mid voltage	Vmin =1.28V Vnorm =1.35V Vmax =1.42V	It must be provided with sufficient current up to 0.4A.
VDD_CORE_VH	46	PI	Voltage for core, high voltage	Vmin =1.85V Vnorm =1.95V Vmax =2.05V	It must be provided with sufficient current up to 0.4A.
VDD_IO	43	PI	Power supply for the module's I/O pins	Vmin =1.7V Vnorm =1.8V Vmax =1.9V	It must be provided with sufficient current up to 0.15A.
VDD_RF	19, 20, 63	PI	Power supply for the module's RF part	Vmin =3.3V Vnorm =3.85V Vmax =4.25V	It must be provided with sufficient current up to 2.0A.
GND	6, 24, 26, 27, 29, 30, 31, 32, 34, 44, 51, 66, 67,		Ground		

	69, 70, 74, 75, 85~108				
WLAN Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_EN	84	DI	WLAN enable control	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain. Active high. It is suggested to pull down this pin with a 10kΩ resistor.
PCIE_ REFCLK_P	54	AO	PCIe reference clock (+)		Require differential impedance of 85Ω.
PCIE_ REFCLK_M	9	AO	PCIe reference clock (-)		
PCIE_TX_P	52	AO	PCIe transmit (+)		
PCIE_TX_M	7	AO	PCIe transmit (-)		
PCIE_RX_P	56	AI	PCIe receive (+)		
PCIE_RX_M	11	AI	PCIe receive (-)		
PCIE_ CLKREQ_N	12	DO	PCIe clock request	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain
PCIE_ RST_N	14	DI	PCIe reset	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain
PCIE_ WAKE_N	13	DO	PCIe wakes up host	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain
WLAN_DBG _TXD	21	DO	WLAN debug UART transmit	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
WLAN_DBG _RXD	65	DI	WLAN debug UART receive	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain. If unused, keep this pin open.
WLAN_ GPIO	48	DO	WLAN general-purpose input/output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
WLAN_LED	3	DO	WLAN LED	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.

BT Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_EN	83	DI	BT enable control	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain. Active high. It is suggested to pull down this pin with a 10kΩ resistor.
PCM_DIN	76	DI	PCM data input	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain.
PCM_SYNC	35	DI	PCM data frame sync	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain.
PCM_CLK	37	DI	PCM clock	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain.
PCM_DOUT	36	DO	PCM data output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
BT_RTS	77	DO	BT UART request to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
BT_CTS	38	DI	BT UART clear to send	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain.
BT_TXD	39	DO	BT UART transmit	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
BT_RXD	78	DI	BT UART receive	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain.
BT_DBG_TXD	23	DO	BT debug UART transmit	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
BT_DBG_RXD	22	DI	BT debug UART receive	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain. If unused, keep this pin open.
Control Signal Pins					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SW_CTRL	57	DO	Switch control	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
Coexistence Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
COEX_TXD	59	DO	LTE/WLAN&BT coexistence transmit	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
COEX_RXD	16	DI	LTE/WLAN&BT coexistence receive	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain. If unused, keep this pin open.
LAA_AS_EN	82	DI	Allow LAA to control WLAN FEM during WLAN sleep mode	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain. If unused, keep this pin open.
LAA_TXEN	41	DI	WLAN XFEM control LAA TX enable	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain. If unused, keep this pin open.
LAA_RX	81	DI	WLAN XFEM control for LAA receiver	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain. If unused, keep this pin open.
WLAN_ TXEN	42	DO	WLAN XFEM control for WLAN TX enable	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
PA_MUTE	80	DI	WLAN XFEM control to disable WLAN PA	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain. If unused, keep this pin open.
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_WIFI0	28	IO	BT and 2G&5G WLAN antenna interface 0		50Ω impedance
ANT_WIFI1	33	IO	2G&5G WLAN antenna interface 1		50Ω impedance
ANT_BT	25	IO	Reserved dedicated		50Ω impedance

			BT antenna interface		
WLAN_SLP_CLK Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	15	DI	Used as a timer in low power modes. External 32.768KHz clock input is required in sleep mode.	V_{IL}min=-0.3V V_{IL}max=0.63V V_{IH}min=1.17V V_{IH}max=2.1V	1.8V power domain. If unused, keep this pin open.
RESERVED Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	4, 5, 8, 10, 17, 18, 40, 49, 50, 53, 55, 58, 60, 61, 62, 64, 68, 71~73, 79		Reserved		Keep these pins open.

NOTE

Please keep all RESERVED and unused pins open.

3.4. Power Supply

The following table shows the power supply pins and ground pins of FG50V module.

Table 4: Definition of Power Supply and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VDD_CORE_VL	1, 2, 47	Voltage for Core, low voltage	0.9	0.95	1.0	V
VDD_CORE_VM	45	Voltage for Core, mid voltage	1.28	1.35	1.42	V
VDD_CORE_VH	46	Voltage for Core, high voltage	1.85	1.95	2.05	V
VDD_IO	43	Power supply for the module's I/O pins	1.7	1.8	1.9	V
VDD_RF	19, 20, 63	Power supply for the module's RF part	3.3	3.85	4.25	V
GND	6, 24, 26, 27, 29, 30, 31, 32, 34, 44, 51, 66, 67, 69, 70, 74, 75, 85~108	Ground				

The VDD_CORE_VL, VDD_CORE_VM, VDD_CORE_VH, and VDD_IO can be powered by RG500Q module, as the following figure shows.

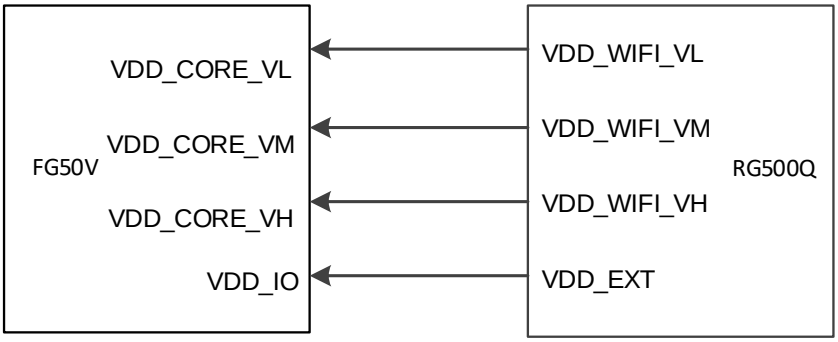


Figure 3: Reference Circuit for VDD_CORE_VL, VDD_CORE_VM, VDD_CORE_VH, and VDD_IO

FG50V module is powered by VDD_RF, and it is recommended to use a power supply chip, which is able to output a current of 2.0A at least.

The following figure shows a reference design for VDD_RF which is controlled by WLAN_PWR_EN1 of RG500Q. WLAN_PWR_EN1 of TPS62130A-Q1 should be connected to the pin 216 (WLAN_PWR_EN1) of RG500Q module. For more details, please refer to ***document [3]***.

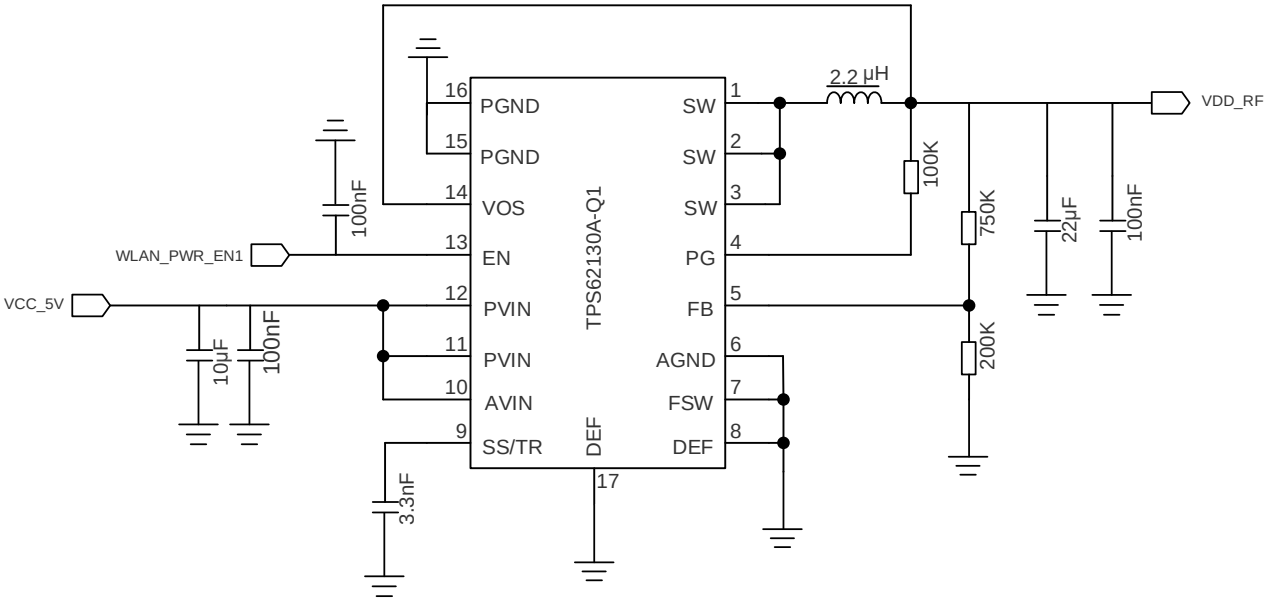


Figure 4: Reference Circuit for VDD_RF

NOTE

AT+QWIFI=1 command can be used to switch on the power supply (VDD_RF) and enable WLAN function.

3.5. WLAN Interface

The following figure shows the WLAN interface connection between FG50V and RG500Q modules.

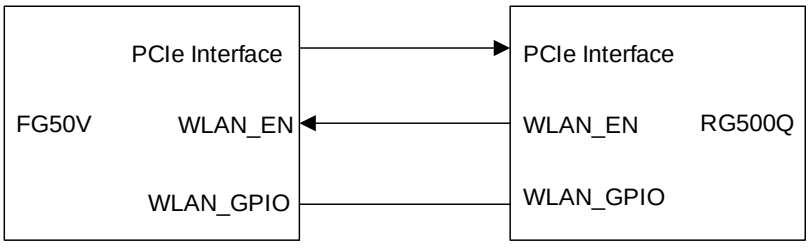


Figure 5: WLAN Interface Connection

3.5.1. WLAN_EN

WLAN_EN is used to control the WLAN function of FG50V module. WLAN function will be enabled when WLAN_EN is at high level.

Table 5: Pin Definition of WLAN_EN

Pin Name	Pin No.	I/O	Description	Comment
WLAN_EN	84	DI	WLAN enable control	Active high

NOTE

WLAN_EN is a sensitive signal, and it should be ground shielded and routed as close as possible to FG50V module.

3.5.2. PCIe Interface

The following table shows the pin definition of the PCIe interface of FG50V.

Table 6: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	54	AO	PCIe reference clock (+)	Require differential impedance of 85Ω.
PCIE_REFCLK_M	9	AO	PCIe reference clock (-)	
PCIE_TX_P	52	AO	PCIe transmit (+)	
PCIE_TX_M	7	AO	PCIe transmit (-)	
PCIE_RX_P	56	AI	PCIe receive (+)	
PCIE_RX_M	11	AI	PCIe receive (-)	
PCIE_CLKREQ_N	12	DO	PCIe clock request	1.8V power domain.
PCIE_RST_N	14	DI	PCIe reset	
PCIE_WAKE_N	13	DO	PCIe wakes up host	

The following figure shows the PCIe interface connection between FG50V and RG500Q modules.

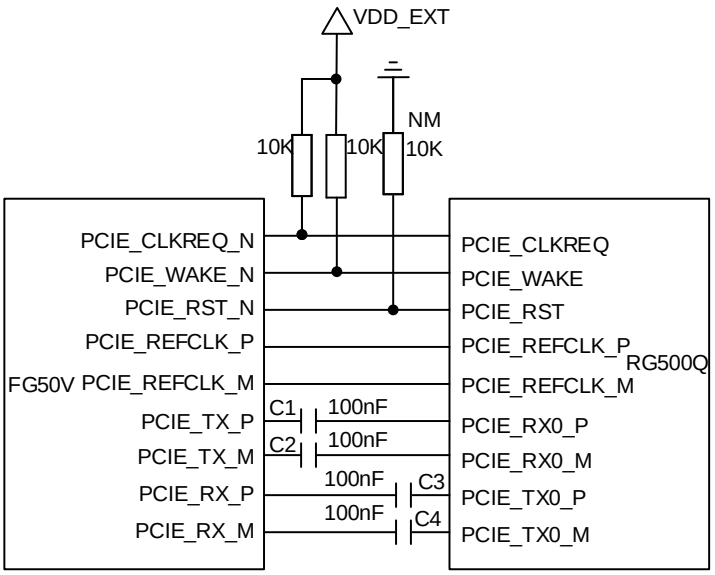


Figure 6: PCIe Interface Connection

In order to ensure the signal integrity of PCIe interface, C1 and C2 should be placed close to the FG50V module, and C3 and C4 should be placed close to the RG500Q module. The extra stubs of traces must be as short as possible.

The following principles of PCIe interface design should be complied with, so as to meet PCIe Gen2 specifications.

- It is important to route the PCIe signal traces as differential pairs with total grounding. And the differential impedance is 85Ω±10%.
- For PCIe signal traces, the maximum length of each differential data pair (TX/RX/REFCLK) is recommended to be less than 300mm, and each differential data pair matching should be less than 0.7mm (5ps).
- Spacing to all other signals (inter-interface) is four times of trace width.
- Do not route signal traces under crystals, oscillators, magnetic devices, or RF signal traces. It is important to route the PCIe differential traces in inner-layer of the PCB and surround the traces with ground on that layer and with ground planes above and below.

3.5.3. WLAN_GPIO and WLAN_LED

Table 7: Pin Definition of WLAN_GPIO and WLAN_LED

Pin Name	Pin No.	I/O	Description	Comment
WLAN_GPIO	48	DO	WLAN general-purpose input/output	1.8V power domain. Under development.
WLAN_LED	3	DO	WLAN LED signal	1.8V power domain. Under development.

NOTE

WLAN_GPIO and WLAN_LED functions of FG50V are still under development.

3.6. BT Interface*

The following figure shows the block diagram of BT interface connection between FG50V and RG500Q modules.

If BT function of FG50V module is used, the UART and PCM interfaces of FG50V must be connected to that of RG500Q module.

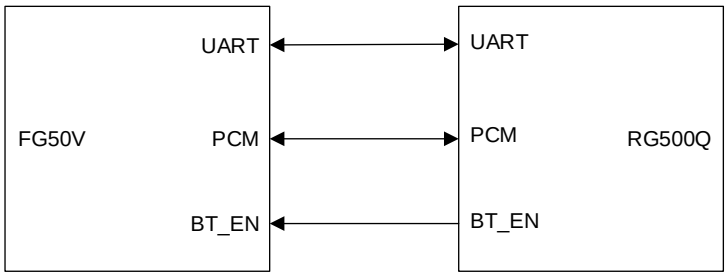


Figure 7: Block Diagram of BT Interface Connection

NOTE

"*" means BT function of FG50V is still under development.

3.6.1. BT_EN

BT_EN is used to control the BT function of FG50V module. BT function will be enabled when BT_EN is at high level.

Table 8: Pin Definition of BT_EN

Pin Name	Pin No.	I/O	Description	Comment
BT_EN	83	DI	Bluetooth enable control	Active high. Under development.

NOTE

BT_EN function of FG50V is still under development.

3.6.2. PCM Interface

The following table shows the pin definition of PCM interface.

Table 9: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	76	DI	PCM data input	1.8V power domain
PCM_SYNC	35	DI	PCM data frame sync	1.8V power domain
PCM_CLK	37	DI	PCM clock	1.8V power domain
PCM_DOUT	36	DO	PCM data output	1.8V power domain

The following figure shows the PCM interface connection between FG50V and RG500Q modules.

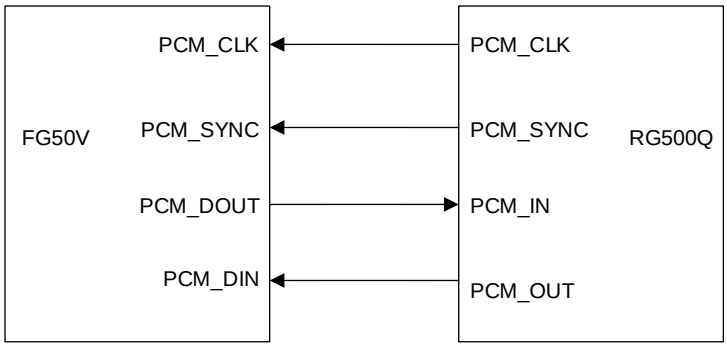


Figure 8: PCM Interface Connection

3.6.3. UART Interface

The following table shows the pin definition of UART interface.

Table 10: Pin Definition of UART Interface

Pin Name	Pin No.	I/O	Description	Comment
BT_RTS	77	DO	BT UART request to send	1.8V power domain
BT_CTS	38	DI	BT UART clear to send	1.8V power domain
BT_TXD	39	DO	BT UART transmit	1.8V power domain
BT_RXD	78	DI	BT UART receive	1.8V power domain

The following figure shows the reference design for UART interface connection between FG50V and RG500Q modules.

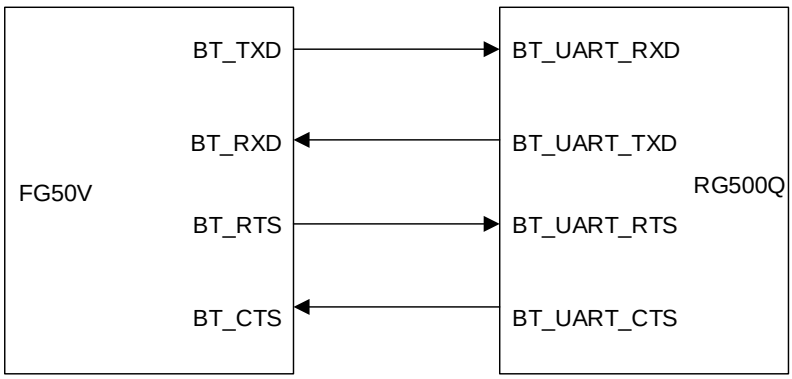


Figure 9: UART Interface Connection

3.7. Control Signal Pins

3.7.1. SW_CTRL

The following table shows the pin definition of SW_CTRL.

Table 11: Pin Definition of SW_CTRL

Pin Name	Pin No.	I/O	Description	Comment
SW_CTRL	57	DO	Switch control	Active high. Under development.

The following figure shows the reference design for SW_CTRL connection between FG50V and RG500Q modules.

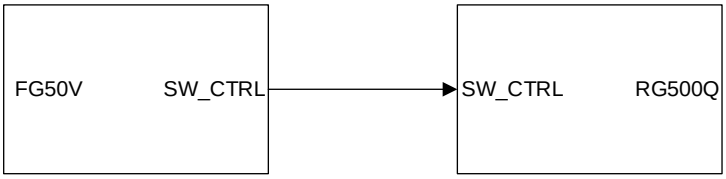


Figure 10: SW_CTRL Connection

NOTE

SW_CTRL function of FG50V is still under development.

3.8. Coexistence Interfaces

3.8.1. UART Coexistence Interface

The following table shows the pin definition of UART coexistence interface.

Table 12: Pin Definition of UART Coexistence Interface

Pin Name	Pin No.	I/O	Description	Comment
COEX_TXD	59	DO	LTE/WLAN&BT coexistence transmit	If unused, keep this pin open.
COEX_RXD	16	DI	LTE/WLAN&BT coexistence receive	If unused, keep this pin open.

FG50V module supports LTE&WLAN coexistence and LTE&BT coexistence. The following figure shows the UART coexistence interface connection between FG50V and RG500Q modules.

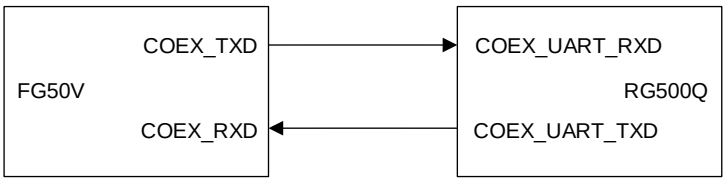


Figure 11: UART Coexistence Interface Connection

3.8.2. Other Coexistence Interfaces*

The following table shows the pin definition of other coexistence interfaces.

Table 13: Pin Definition of Other Coexistence Interface

Pin Name	Pin No.	I/O	Description	Comment
LAA_AS_EN	82	DI	Allow LAA to control WLAN FEM during WLAN sleep mode	If unused, keep this pin open.
LAA_TXEN	41	DI	WLAN XFEM control LAA TX enable	If unused, keep this pin open.
LAA_RX	81	DI	WLAN XFEM control for LAA receiver	If unused, keep this pin open.
WLAN_TXEN	42	DO	WLAN XFEM control for WLAN TX enable	If unused, keep this pin open.
PA_MUTE	80	DI	WLAN XFEM control to disable WLAN PA	If unused, keep this pin open.

NOTE

"*" means other coexistence interfaces of FG50V are still under development.

3.9. WLAN_SLP_CLK Interface*

The 32.768KHz clock is used in low power modes, such as IEEE power saving mode and sleep mode. It serves as a timer to determine when to wake up FG50V module to receive signals in various power saving schemes, and to maintain basic logic operations when the module is in sleep mode.

Table 14: Pin Definition of WLAN_SLP_CLK Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK	15	DI	External 32.768KHz clock input is required in sleep mode.	If unused, keep this pin open.

NOTE

"*" means sleep mode function of FG50V is still under development.

3.10. RF Antenna Interfaces

The following table shows the pin definition of RF antenna interfaces.

Table 15: Pin Definition of RF Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI0	28	IO	BT and 2G&5G WLAN antenna interface 0	50Ω impedance
ANT_WIFI1	33	IO	2G&5G WLAN antenna interface 1	50Ω impedance
ANT_BT	25	IO	Reserved dedicated BT antenna interface	50Ω impedance

3.10.1. Operating Frequency

Table 16: Operating Frequency of the Module

Feature	Frequency	Unit
2.4GHz WLAN	2.412~2.472	GHz
5GHz WLAN	5.180~5.825	GHz
BT	2.402~2.480	GHz

3.10.2. Reference Design of RF Antenna Interfaces

FG50V module provides three RF antenna interfaces for antenna connection. A reference circuit design for an RF antenna interface is shown below.

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (C1, C2, R1) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

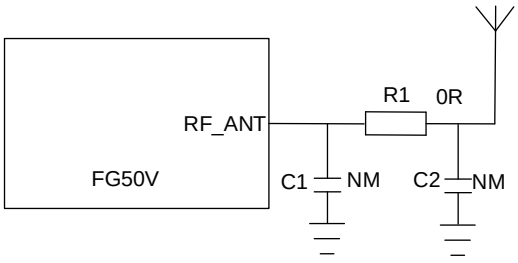


Figure 12: Reference Circuit for RF Antenna Interfaces

3.10.3. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

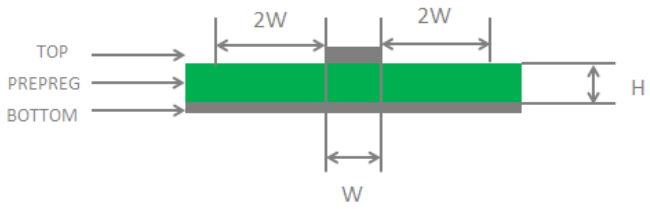


Figure 13: Microstrip Design on a 2-layer PCB

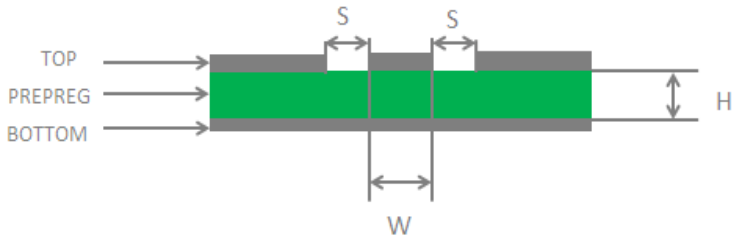


Figure 14: Coplanar Waveguide Design on a 2-layer PCB

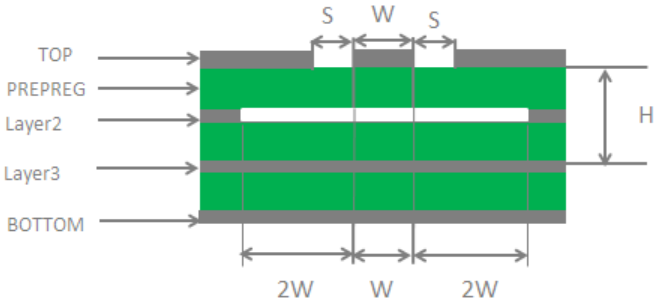


Figure 15: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

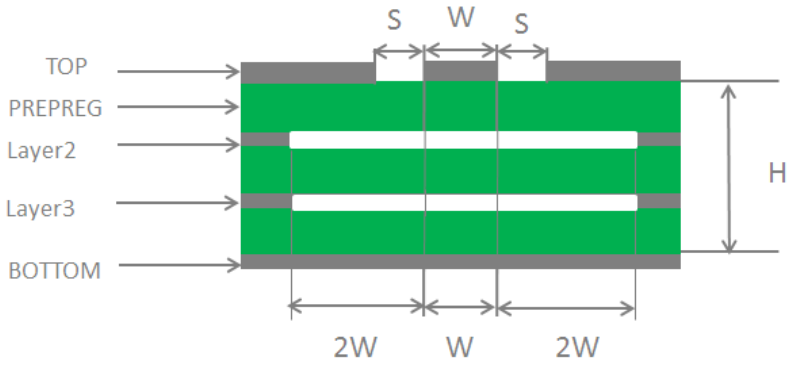


Figure 16: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, ground vias around RF traces and the reference ground improves RF performance. The distance between the ground vias and RF traces should be more than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [4]***.

3.10.4. Antenna Requirements

The following tables show the requirements on antenna cables and antennas.

Table 17: Antenna Cable Requirements

Type	Requirements
2.412GHz~2.472GHz	Cable insertion loss <1dB
5.180GHz~5.825GHz	Cable insertion loss <1dB

Table 18: Antenna Requirements

Type	Requirements
Frequency Range	2.412GHz~2.472GHz 5.180GHz~5.825GHz
VSWR	< 2:1 recommended
Gain (dBi)	Typical 1
Max Input Power (W)	50
Input Impedance (Ω)	50
Polarization Type	Vertical

3.10.5. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

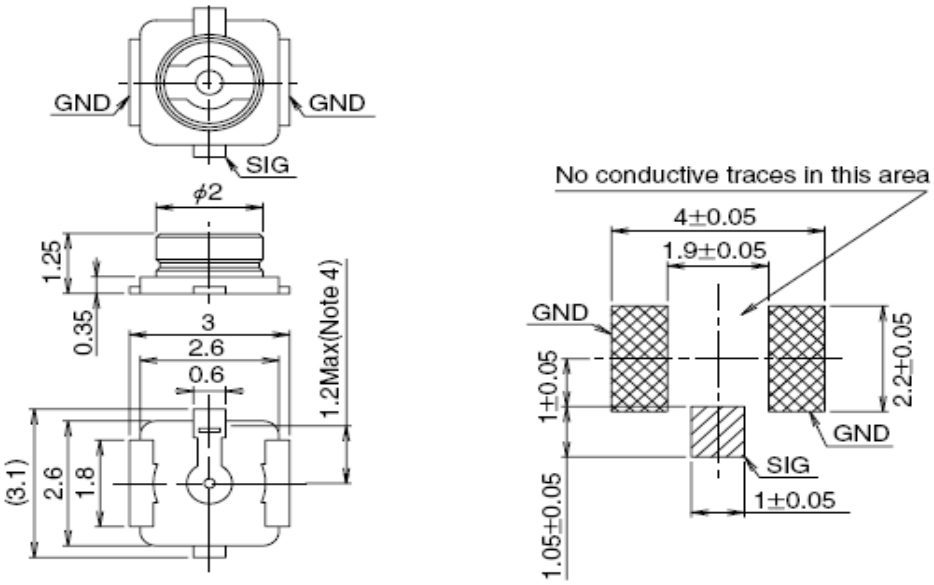


Figure 17: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

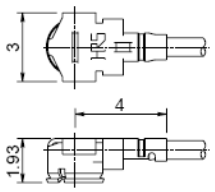
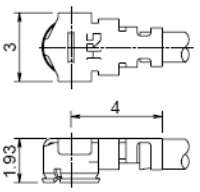
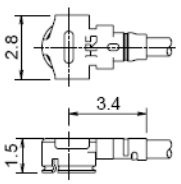
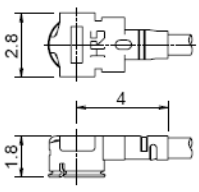
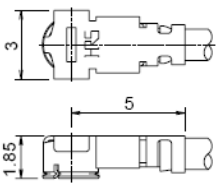
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 18: Mechanicals of UF.L-LP Connectors (Unit: mm)

The following figure describes the space factor of mated connector

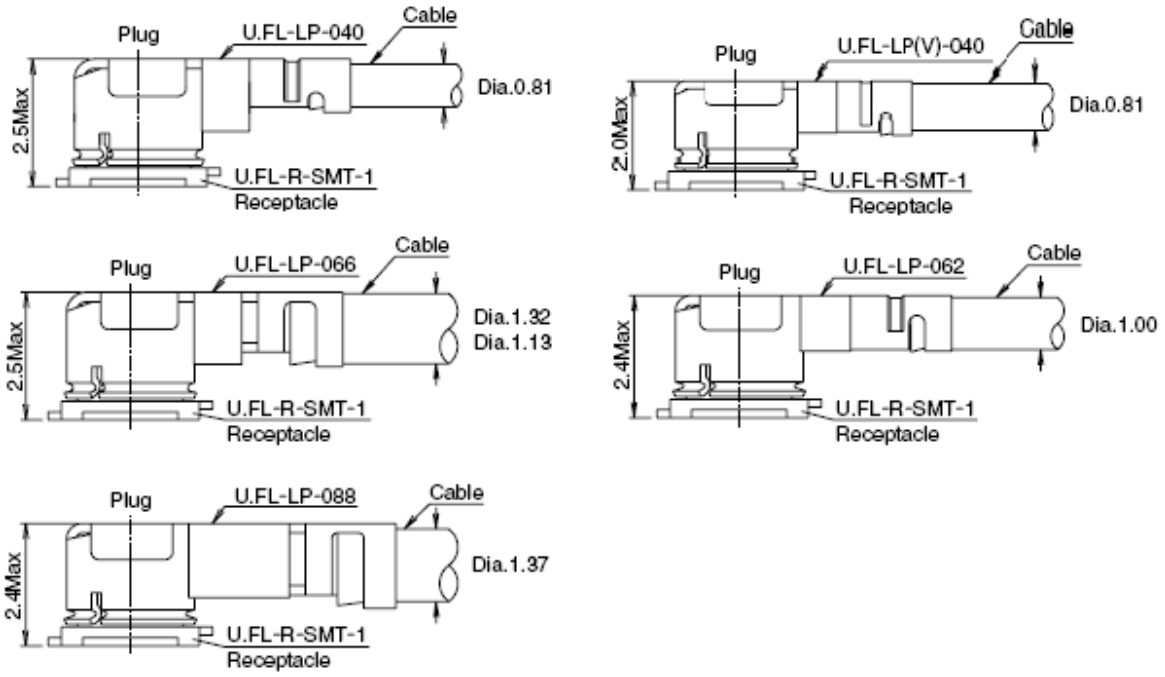


Figure 19: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

4 Electrical, Reliability and Radio Characteristics

4.1. General Description

This chapter mainly introduces electrical and radio frequency characteristics of FG50V module. The details are listed in the subsequent chapters.

4.2. Electrical Characteristics

The following table shows the absolute maximum ratings.

Table 19: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VDD_CORE_VL	-0.3	V_{DDX}+0.2	V
VDD_CORE_VM	-0.3	V_{DDX}+0.2	V
VDD_CORE_VH	-0.3	V_{DDX}+0.2	V
VDD_IO	-0.3	V_{DDX}+0.2	V
VDD_RF	3.0	4.8	V
Digital I/O Input Voltage	-0.3	VDD_IO+0.2	V

NOTE

V_{DDX} is the supply voltage associated with the input pin to which the test voltage is applied.

The following table shows the recommended operating conditions of FG50V module.

Table 20: Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
VDD_CORE_VL	0.9	0.95	1.0	V
VDD_CORE_VM	1.28	1.35	1.42	V
VDD_CORE_VH	1.85	1.95	2.05	V
VDD_IO	1.7	1.8	1.9	V
VDD_RF	3.3	3.85	4.25	V

4.3. I/O Interface Characteristics

The following table shows the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 21: General DC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	High Level Input Voltage	0.65 × VDD_IO	VDD_IO+0.3	V
V_{IL}	Low Level Input Voltage	-0.3	0.35 × VDD_IO	V
V_{OH}	High Level Output Voltage	VDD_IO-0.45	VDD_IO	V
V_{OL}	Low Level Output Voltage	0	0.45	V
I_{IL}	Input Leakage Current	TBD	TBD	μA

4.4. Current Consumption

The values of current consumption are shown as below.

Table 22: Current Consumption of the Module (Low Power Modes)

Description	Conditions	I_{WLAN_3V3}	I_{VIO}	Unit
OFF State [1)]	**AT+QWIFI=0**	TBD	TBD	μA
Idle [2)]	**AT+QWIFI=1**	TBD	TBD	mA

Table 23: Current Consumption of the Module (Normal Operation)

Description	Conditions	I_{WLAN_3V3}	Unit
802.11b	TX 1Mbps @17.5dBm	TBD	mA
	TX 11Mbps @17.2dBm	TBD	mA
	RX 1Mbps	TBD	mA
	RX 11Mbps	TBD	mA
802.11g	TX 6Mbps @16dBm	TBD	mA
	TX 54Mbps @14.8dBm	TBD	mA
	RX 6Mbps	TBD	mA
	RX 54Mbps	TBD	mA
802.11n	TX HT20-MCS0 @15.8dBm	TBD	mA
	TX HT20-MCS7 @13.5dBm	TBD	mA
	TX HT40-MCS0 @14.5dBm	TBD	mA
	TX HT40-MCS7 @12.5dBm	TBD	mA
	RX HT20-MCS0	TBD	mA
	RX HT20-MCS7	TBD	mA
	RX HT40-MCS0	TBD	mA
	RX HT40-MCS7	TBD	mA
802.11a	TX 6Mbps @14dBm	TBD	mA
	TX 54Mbps @10dBm	TBD	mA
	RX 6Mbps	TBD	mA

	RX 54Mbps	TBD	mA
802.11ac	TX VHT20 MCS0 @13.5dBm	TBD	mA
	TX VHT20 MCS8 @9dBm	TBD	mA
	TX VHT40 MCS0 @12.5dBm	TBD	mA
	TX VHT40 MCS9 @8dBm	TBD	mA
	TX VHT80 MCS0 @11dBm	TBD	mA
	TX VHT80 MCS9 @7dBm	TBD	mA
	RX VHT20 MCS0	TBD	mA
	RX VHT20 MCS8	TBD	mA
	RX VHT40 MCS0	TBD	mA
	RX VHT40 MCS9	TBD	mA
	RX VHT80 MCS0	TBD	mA
	RX VHT80 MCS9	TBD	mA
802.11ax	RX VHT20 MCS0	TBD	mA
	RX VHT20 MCS8	TBD	mA
	RX VHT40 MCS0	TBD	mA
	RX VHT40 MCS9	TBD	mA
	RX VHT80 MCS0	TBD	mA
	RX VHT80 MCS9	TBD	mA

NOTES

1. [1)] OFF State: **AT+QWIFI=0** command can be used to set the module to OFF state (Wi-Fi disabled). In this state, the sleep clock is disabled and no data is saved.
2. [2)] Idle State: In this state, Wi-Fi enabled with **AT+QWIFI=1** but no device is connected.

4.5. RF Performances

The following tables summarize the transmitting and receiving performances of FG50V.

4.5.1. Conducted RF Output Power

Table 24: Conducted RF Output Power at 2.4GHz

Frequency	Min.	Typ.	Unit
802.11b @1Mbps	17	19.5	dBm
802.11b @11Mbps	17	19.5	dBm
802.11g @6Mbps	15	18.5	dBm
802.11g @54Mbps	14.5	17	dBm
802.11n, HT20 @MCS0	15	18.5	dBm
802.11n, HT20 @MCS11	11	13.5	dBm
802.11ac, HT40 @MCS0	15.5	18	dBm
802.11ac, HT40 @MCS11	10.5	13	dBm
802.11ax, HE40 @MCS0	15.5	18	dBm
802.11ax, HE40 @MCS11	10.5	13	dBm

Table 25: Conducted RF Output Power at 5GHz

Frequency	Min.	Typ.	Unit
802.11g @6Mbps	14	16.5	dBm
802.11g @54Mbps	12	14.5	dBm
802.11ac, VHT20 @MCS0	14	16.5	dBm
802.11ac, VHT20 @MCS11	8.5	11	dBm
802.11ac, VHT40 @MCS0	13.5	16	dBm
802.11ac, VHT40 @MCS11	8	10.5	dBm
802.11ac, VHT80 @MCS0	13	15.5	dBm
802.11ac, VHT80 @MCS11	7.5	10	dBm
802.11ax, VHT20 @MCS0	14	16.5	dBm

802.11ax, VHT20 @MCS11	8.5	11	dBm
802.11ax, VHT40 @MCS0	13.5	16	dBm
802.11ax, VHT40 @MCS11	8	10.5	dBm
802.11ax, VHT80 @MCS0	13	15.5	dBm
802.11ax, VHT80 @MCS11	7.5	10	dBm

4.5.2. Conducted RF Receiving Sensitivity

Table 26: Conducted RF Receiving Sensitivity at 2.4GHz

Frequency	Receiving Sensitivity (Typ.)
802.11b, 1Mbps	-94dBm
802.11b, 11 Mbps	-92dBm
802.11g, 6Mbps	-88dBm
802.11g, 54Mbps	-77dBm
802.11n, HT20, MCS0	-89dBm
802.11n, HT20, MCS7	-73dBm
802.11n, HT40, MCS0	-85dBm
802.11n, HT40, MCS7	-70dBm

Table 27: Conducted RF Receiving Sensitivity at 5GHz

Frequency	Receiving Sensitivity (Typ.)
802.11a, 6Mbps	-90dBm
802.11a, 54Mbps	-72dBm
802.11ac, VHT20, MCS0	-90dBm
802.11ac, VHT20, MCS8	-70dBm
802.11ac, VHT40, MCS0	-87dBm

802.11ac, VHT40, MCS9	-65dBm
802.11ac, VHT80, MCS0	-84dBm
802.11ac, VHT80, MCS9	-63dBm
802.11ax, HE20, MCS0	-90dBm
802.11aX, HE20, MCS8	-70dBm
802.11ax, HE40, MCS0	-87dBm
802.11ax, HE40, MCS9	-65dBm
802.11ax, HE80, MCS0	-84dBm
802.11ax, HE80, MCS9	-63dBm

4.6. Electrostatic Discharge

The module is not protected against Electrostatic Discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

5 Mechanical Dimensions

This chapter describes the mechanical dimensions of FG50V module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05mm unless otherwise specified.

5.1. Mechanical Dimensions of the Module

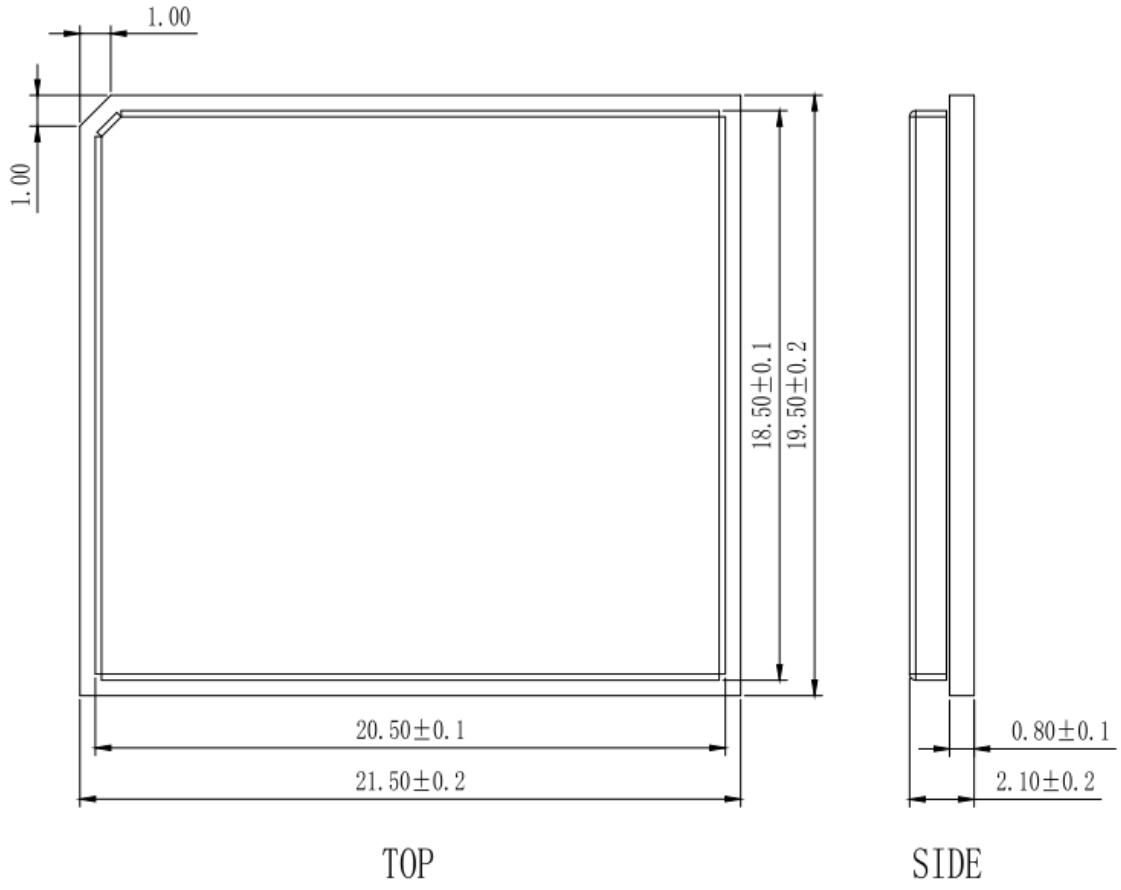


Figure 20: FG50V Top and Side Dimensions

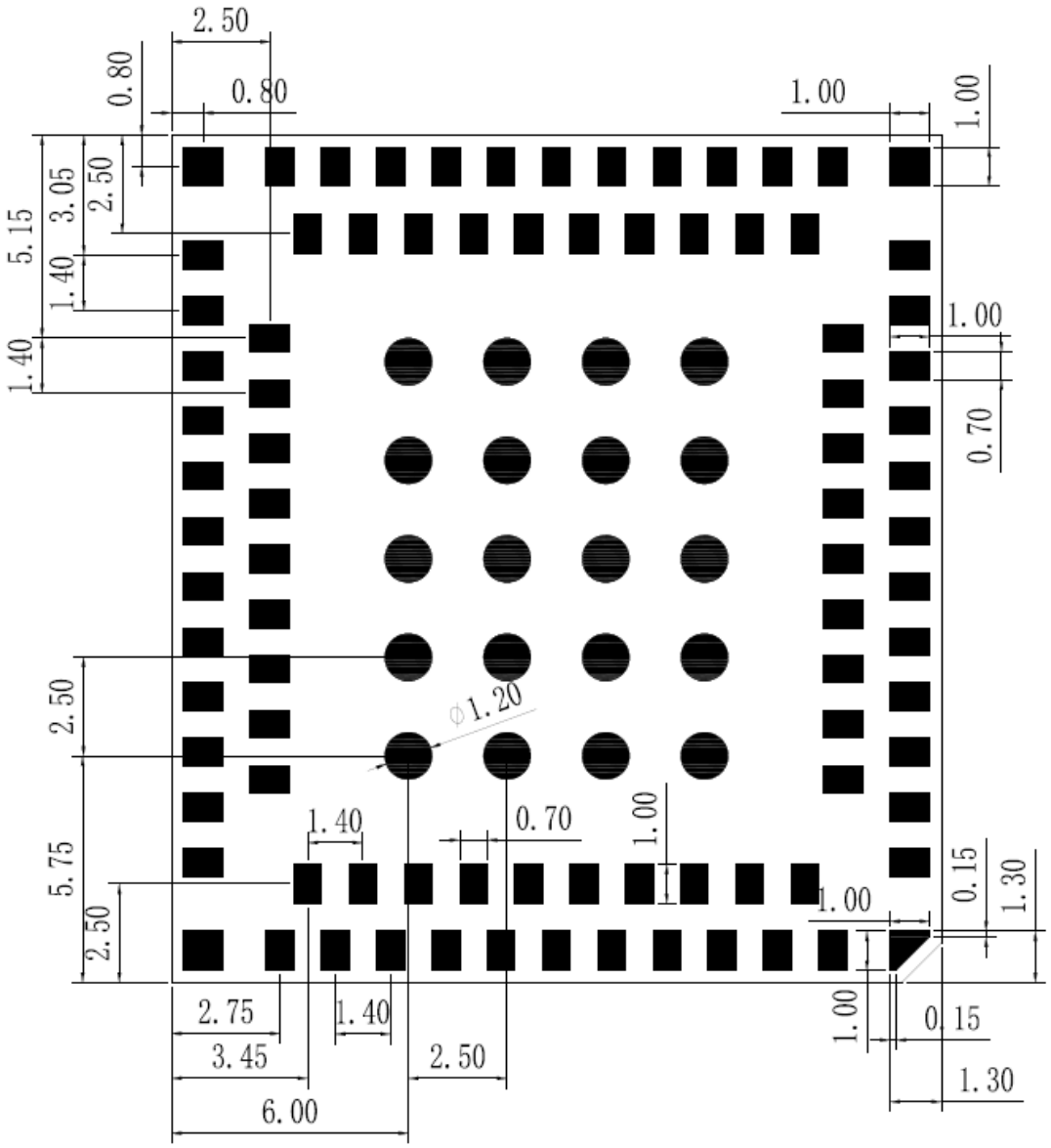


Figure 21: FG50V Bottom Dimension (Bottom View)

5.2. Recommended Footprint

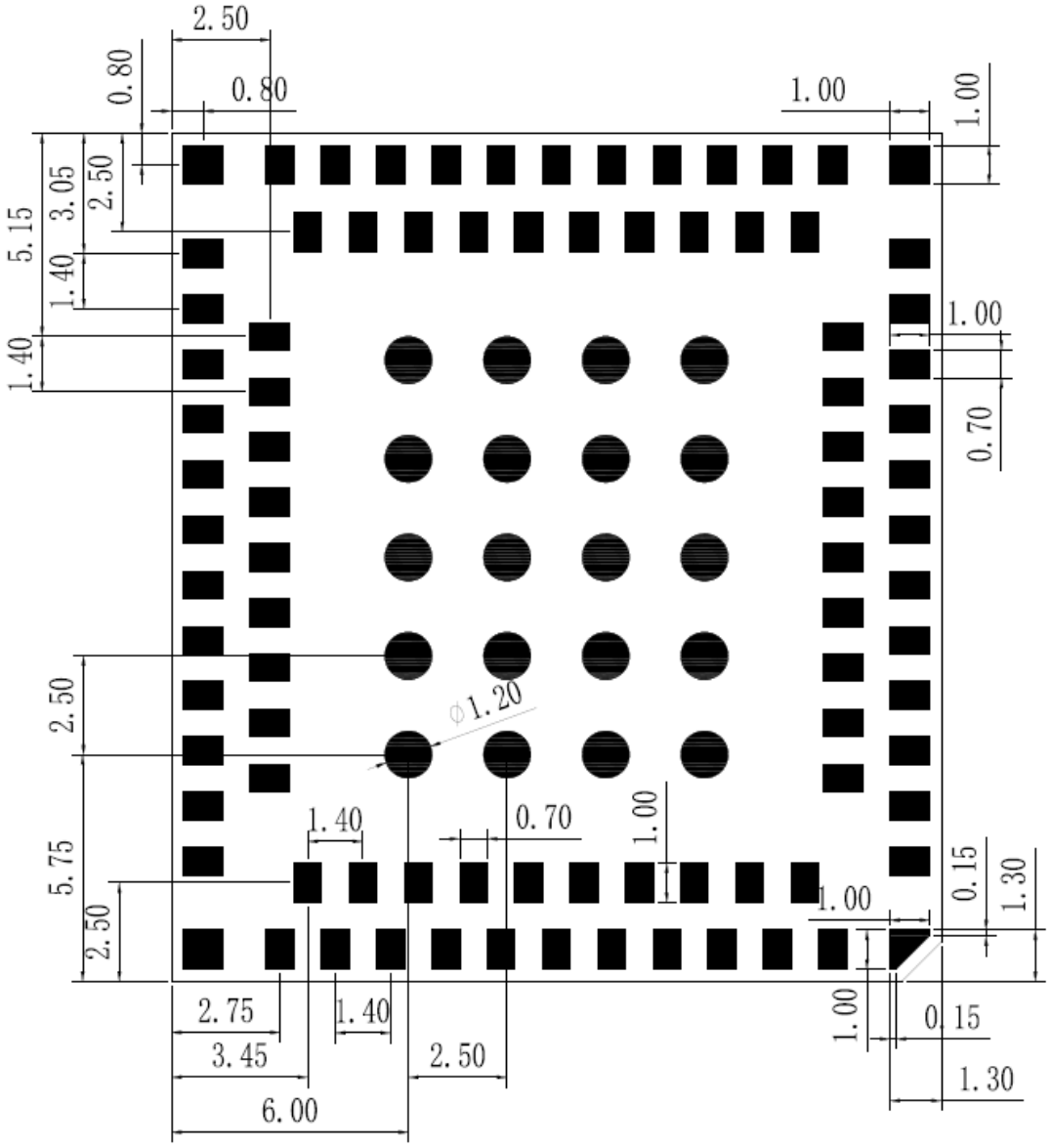


Figure 22: Recommended Footprint (Bottom View)

NOTES

1. For easy maintenance of the module, please keep about 3mm spaces between the module and other components on host PCB.
2. Keep all RESERVED pins open.

5.3. Top and Bottom Views of the Module

Figure 23: Top View of the Module

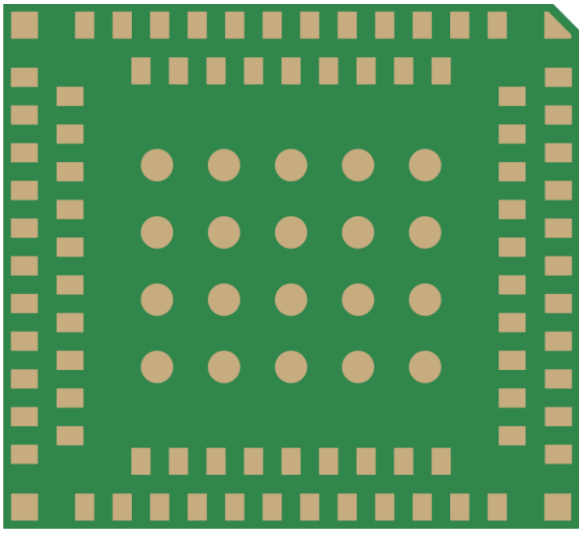


Figure 24: Bottom View of the Module

NOTE

These are renderings of FG50V module. For authentic appearance, please refer to the module that you receive from Quectel.

6 Storage, Manufacturing and Packaging

6.1. Storage

FG50V is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at < 40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:

   - Mounted within 168 hours at the factory environment of ≤ 30ºC/60%RH.
   - Stored at <10% RH.

3. Devices require baking before mounting, if any circumstance below occurs:

   - When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤ 30ºC/60% RH.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

6.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13mm~0.15mm. For more details, please refer to ***document [5]***.

It is suggested that the peak reflow temperature is 238~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

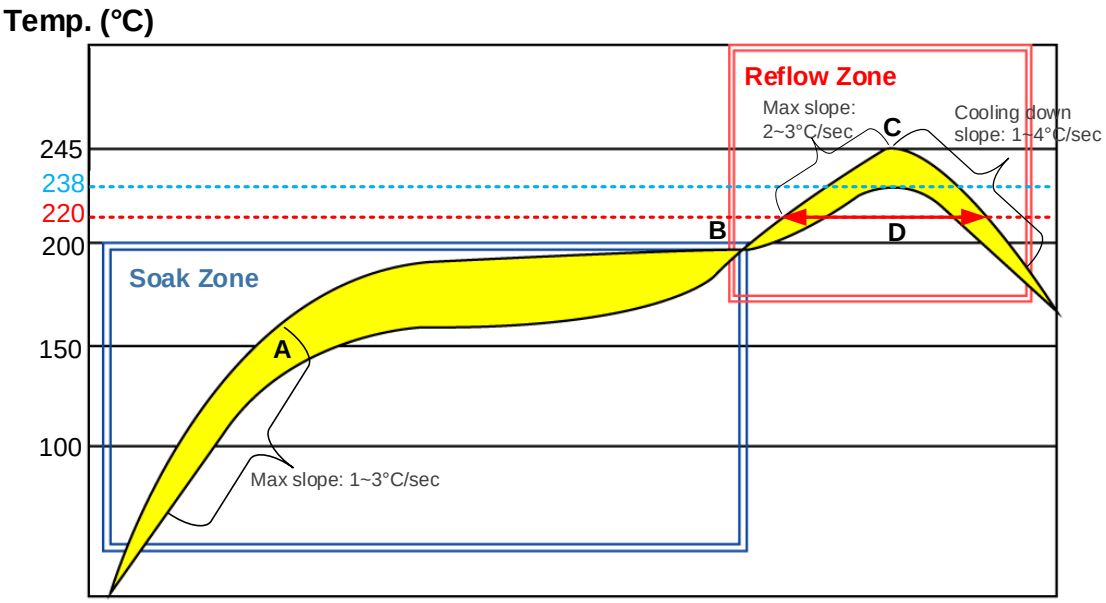


Figure 25: Recommended Reflow Soldering Thermal Profile

Table 28: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec
Reflow Zone	

Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	238°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

6.3. Packaging

FG50V module is packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

FG50V is packaged in tape and reel carriers.

Table 29: Reel Packaging

Model Name	MOQ for MP	Minimum Package: TBD	Minimum Package TBD
FG50V	TBD	Size: TBD N.W: TBD G.W: TBD	Size: TBD N.W: TBD G.W: TBD

7 Appendix A References

Table 30: Related Documents

SN	Document Name	Remark
[1]	Quectel_LTE_OPEN_EVB_User_Guide	EVB user guide for Quectel LTE-QuecOpen modules
[2]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB user guide
[3]	Quectel_RG500Q_Reference_Design	RG500Q reference design
[4]	Quectel_RF_Layout_Application_Note	RF layout application note
[5]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide

Table 31: Terms and Abbreviations

Abbreviation	Description
AP	Access Point
BPSK	Binary Phase Shift Keying
BT	Bluetooth
CCK	Complementary Code Keying
CTS	Clear To Send
ESD	Electrostatic Discharge
GND	Ground
HT	High Throughput
IEEE	Institute of Electrical and Electronics Engineers
I_{IL}	Input Leakage Current
I/O	Input/Output

LTE	Long Term Evolution
Mbps	Megabits per second
MCS	Modulation and Coding Scheme
MOQ	Minimum Order Quantity
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RH	Relative Humidity
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
RX	Receive
SDIO	Secure Digital Input/Output
TBD	To Be Determined
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VHT	Very High Throughput
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value

VSWR	Voltage Standing Wave Ratio
Wi-Fi	Wireless-Fidelity
WLAN	Wireless Local Area Network