EC200S-CN

Reference Design

LTE Standard Module Series

Rev. EC200S-CN_Reference_Design_V1.1

Date: 2020-07-16

Status: Released

Our aim is to provide customers with timely and comprehensive service. For any assistance, please contact our company headquarters:

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GENERAL NOTES

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About the Document

Revision History

Version	Date	Author	Description
1.0	2020-04-12	Vane WANG	Initial
1.1	2020-07-16	Vane WANG	1. Updated the recommended module power supply current to 3.0 A (Sheet 1, 2 and 5). 2. Added audio power amplifier circuit of module analog audio interface (Sheet 11).

Contents

1 Reference Design

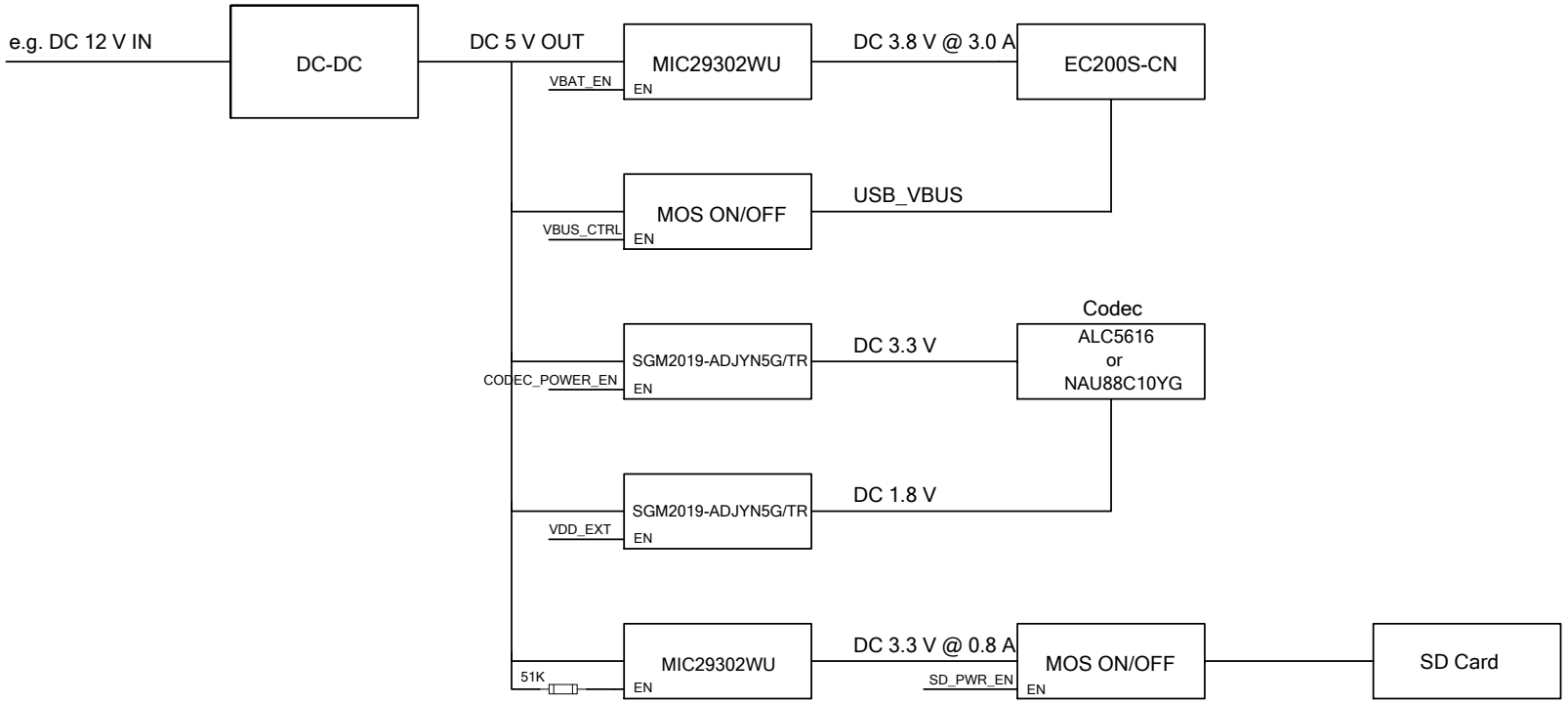
1.1. Introduction

This document provides the reference design for Quectel EC200S-CN module. And the reference design includes block diagrams, power supply, audio interfaces, UART interfaces, (U)SIM interface, SD card interface, etc.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Power Supply Block Diagram



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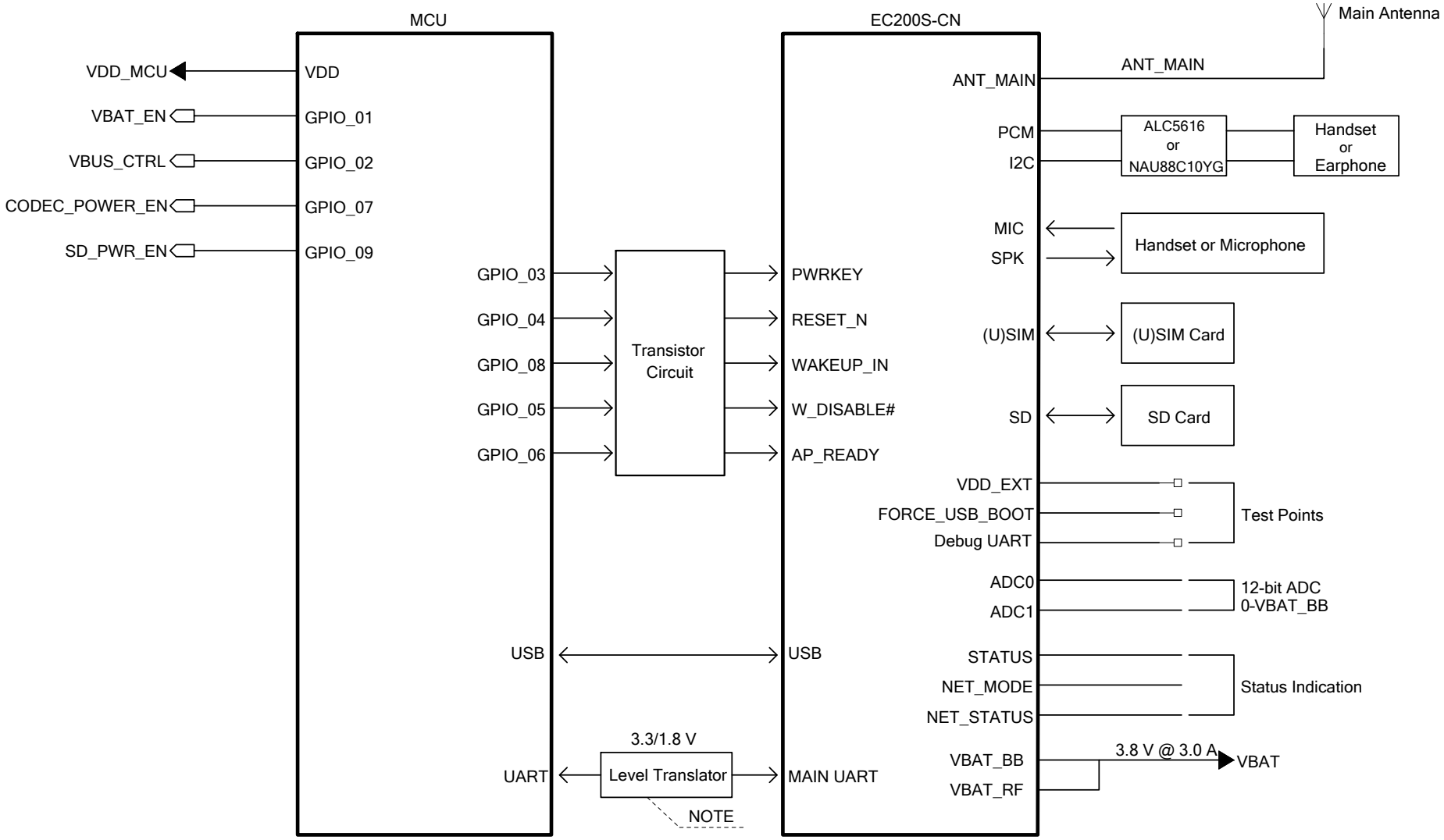
	SHEET 1 OF 14	DATE 2020/7/16

Reference Design Block Diagram



NOTE:
A transistor translation circuit or a level translator TXS0108EPWR provided by Texas Instruments is recommended.

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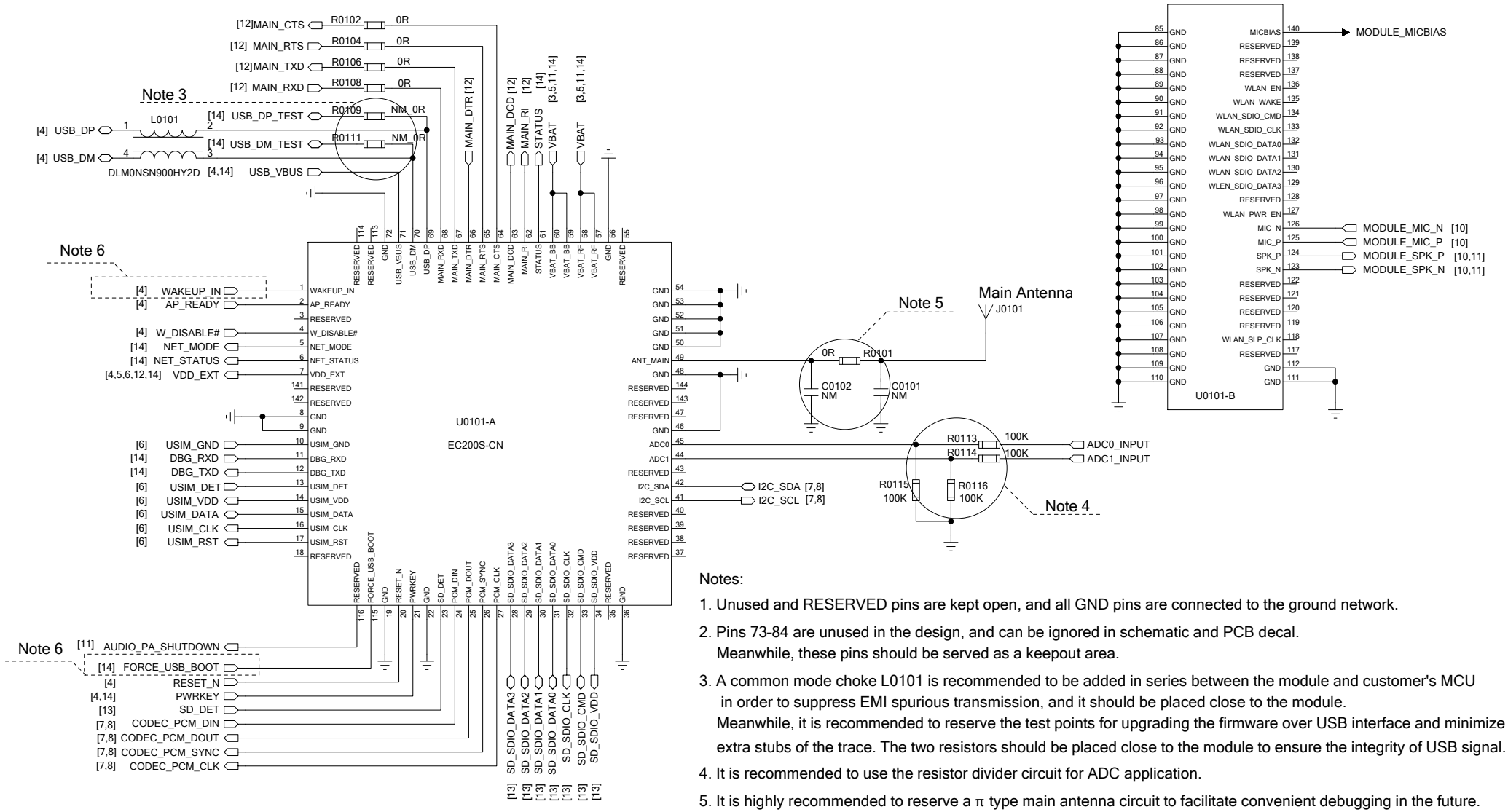
	SHEET 2 OF 14	DATE 2020/7/16

Module Interface



Notes:

1. Unused and RESERVED pins are kept open, and all GND pins are connected to the ground network.
2. Pins 73-84 are unused in the design, and can be ignored in schematic and PCB decal.
   Meanwhile, these pins should be served as a keepout area.
3. A common mode choke L0101 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission, and it should be placed close to the module.
   Meanwhile, it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace. The two resistors should be placed close to the module to ensure the integrity of USB signal.
4. It is recommended to use the resistor divider circuit for ADC application.
5. It is highly recommended to reserve a π type main antenna circuit to facilitate convenient debugging in the future.
   The impedance of the RF signal traces must be controlled as 50 Ω when routing.
6. FORCE_USB_BOOT and WAKEUP_IN cannot be pulled up before startup.

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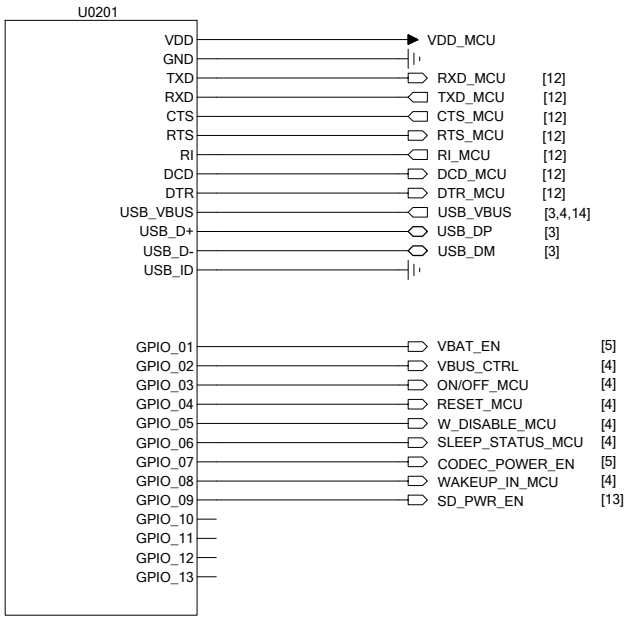
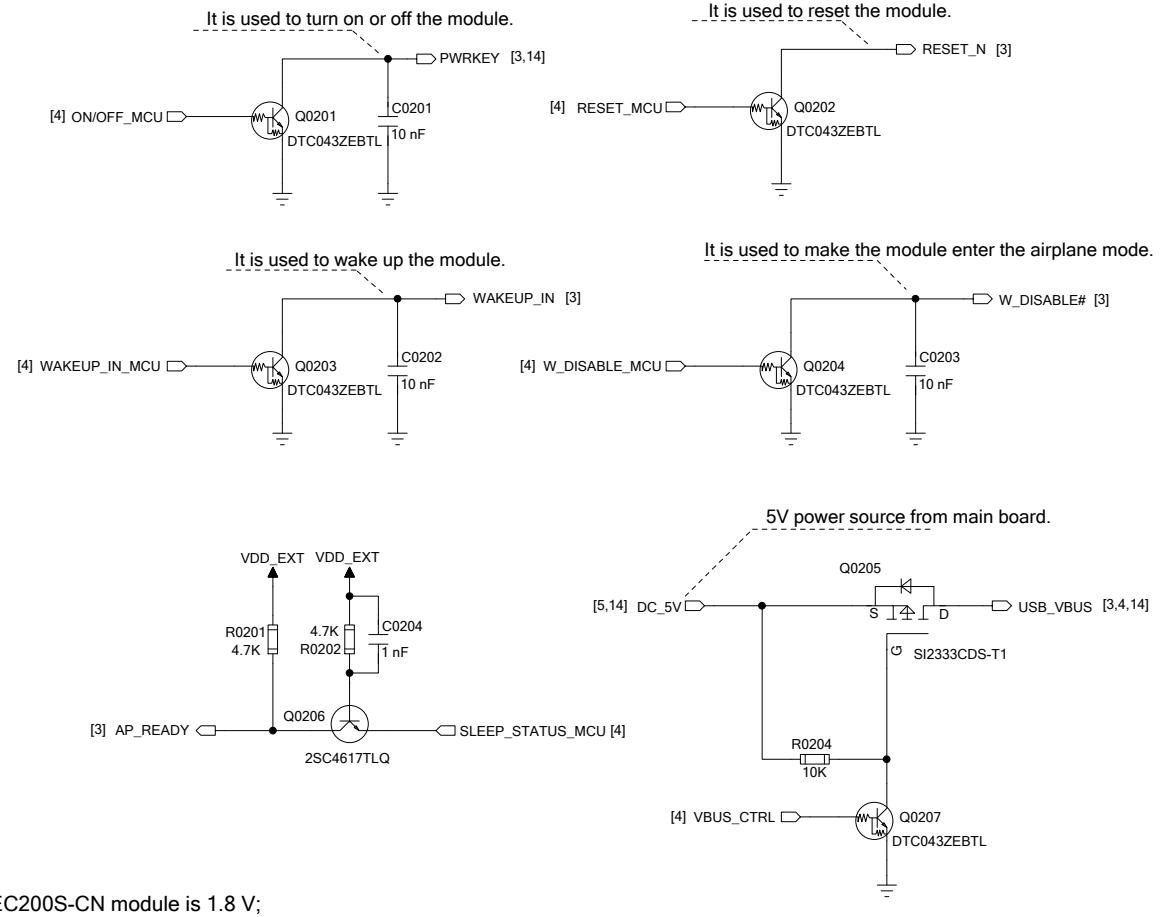
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 3 OF 14	DATE 2020/7/16

MCU Interface





Notes:

1. U0201 represents customer's MCU. The power domain of GPIO interfaces of EC200S-CN module is 1.8 V;
   if the GPIO interfaces of U0201 share the same power domain, then the related level translation circuit can be omitted.
2. The USB interface of EC200S-CN can only serves as a slave device and supports Full-speed and High-speed modes.
   To communicate with the USB interface, MCU needs to support USB host or OTG function. The USB_VBUS pin of the module
   should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the default low-level GPIO pins of MCU as the control pins for PWRKEY and RESET_N of the module.
   Please ensure that there is no large load capacitance with the max value exceeding 10nF on PWRKEY and RESET_N pins.

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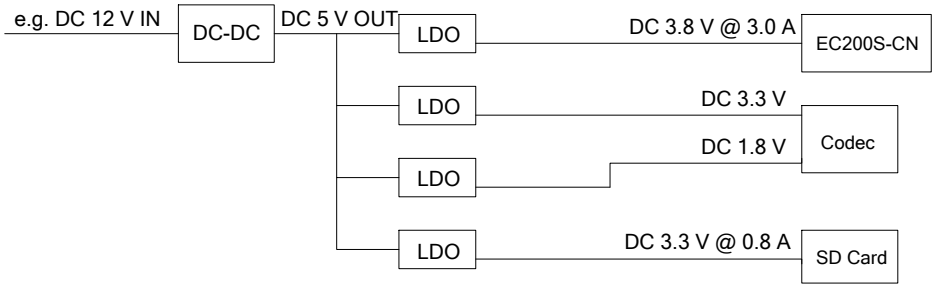
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 4 OF 14	DATE 2020/7/16

Power Supply Design

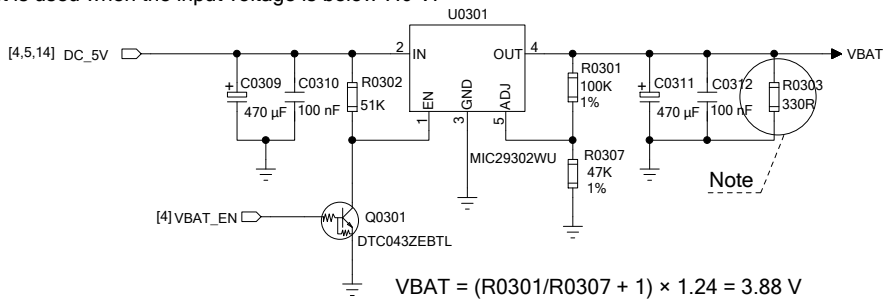
DC-DC Application

It is used when the input voltage is above 7.0 V. Use a DC-DC converter to convert a high input voltage into a 5.0 V output, and then the LDOs will generate 3.8 V, 3.3 V and 1.8 V typical voltages.



LDO Application

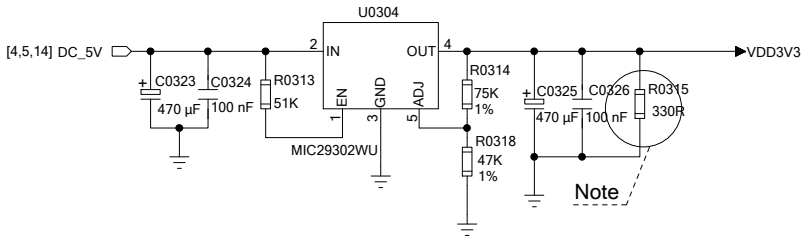
It is used when the input voltage is below 7.0 V.



VBAT = (R0301/R0307 + 1) × 1.24 = 3.88 V

Note: The recommended load current is greater than 10 mA.

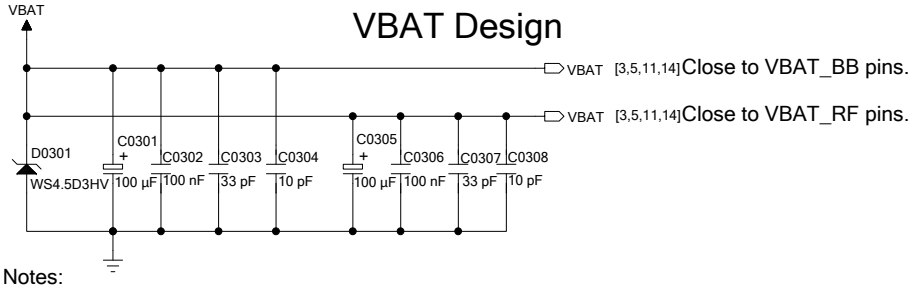
Power Supply for SD Card



VDD3V3 = (R0314/R0318 + 1) × 1.24 = 3.3 V

Note: The recommended load current is greater than 10 mA.

VBAT Design

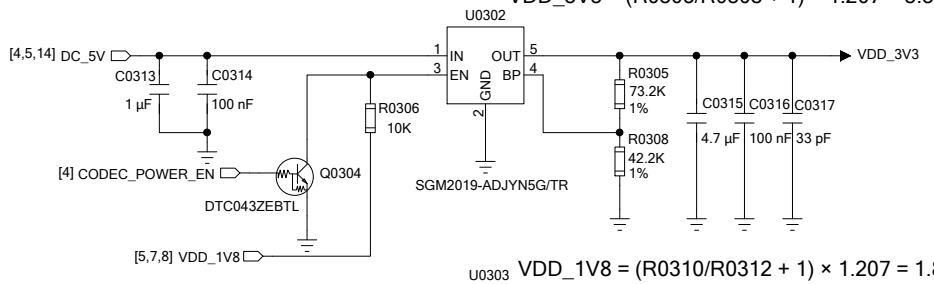


Notes:

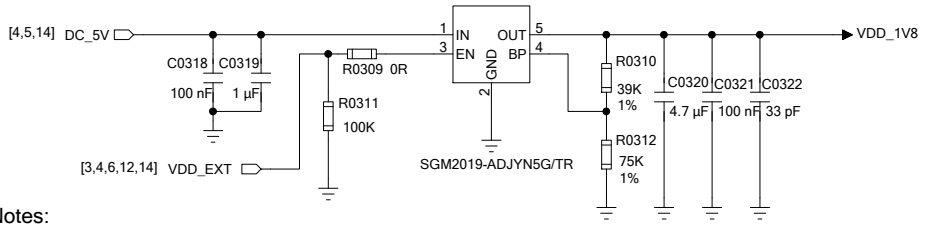
1. The power supply must be able to provide sufficient current up to 3.0 A or more.
2. VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.4-4.5 V.

Power Supply for PCM Codec

VDD_3V3 = (R0305/R0308 + 1) × 1.207 = 3.3 V



VDD_1V8 = (R0310/R0312 + 1) × 1.207 = 1.8 V



Notes:

1. CODEC_POWER_EN must be at a low level in order to ensure the normal output voltage of VDD_3V3. If VDD_3V3 power supply needs to be switched off, please keep CODEC_POWER_EN at a high level.
2. The following power-on/off sequences should be followed to ensure the audio codec works normally.
   Power-on Sequence: power on VDD_1V8 first, then VDD_3V3.
   Power-off Sequence: power off VDD_3V3 first, then VDD_1V8.

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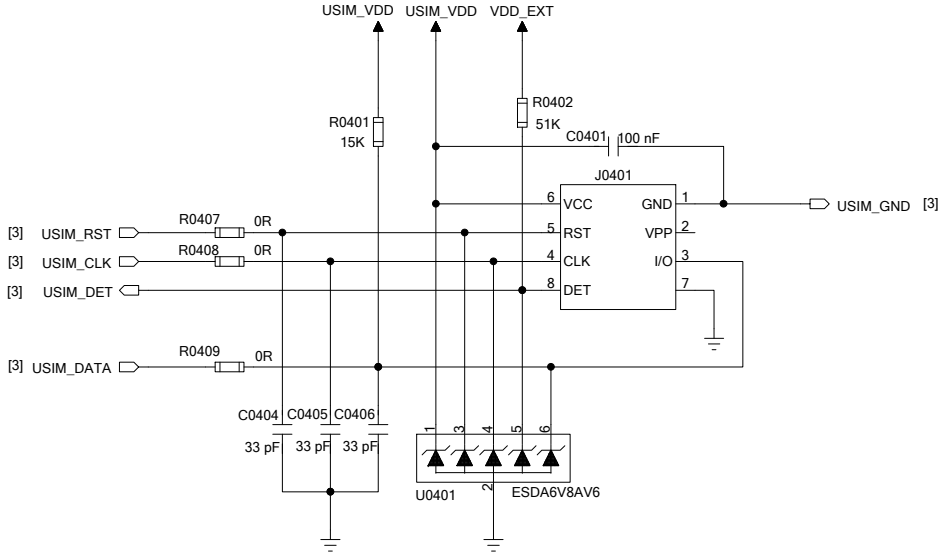
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 5 OF 14	DATE 2020/7/16

(U)SIM Interface Design



Notes:

1. U0401 is recommended to be used to offer good ESD protection, and the parasitic capacitance should not be more than 15 pF.
2. The GND of the (U)SIM card connector is recommended to be connected to the module's USIM_GND. In addition, it can be connected to the GND of customers' PCB directly if the PCB's GND is complete.
3. The pull-up resistor R0401 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
4. R0407-R0409 are used for debugging, and C0404-C0406 are used for filtering interference of EGSM900.
5. C0401's capacitance should be less than 1 μF and it should be placed close to the (U)SIM card connector.
6. For more information about the layout of (U)SIM interface, please refer to *Quectel_EC200S-CN_Hardware_Design.*

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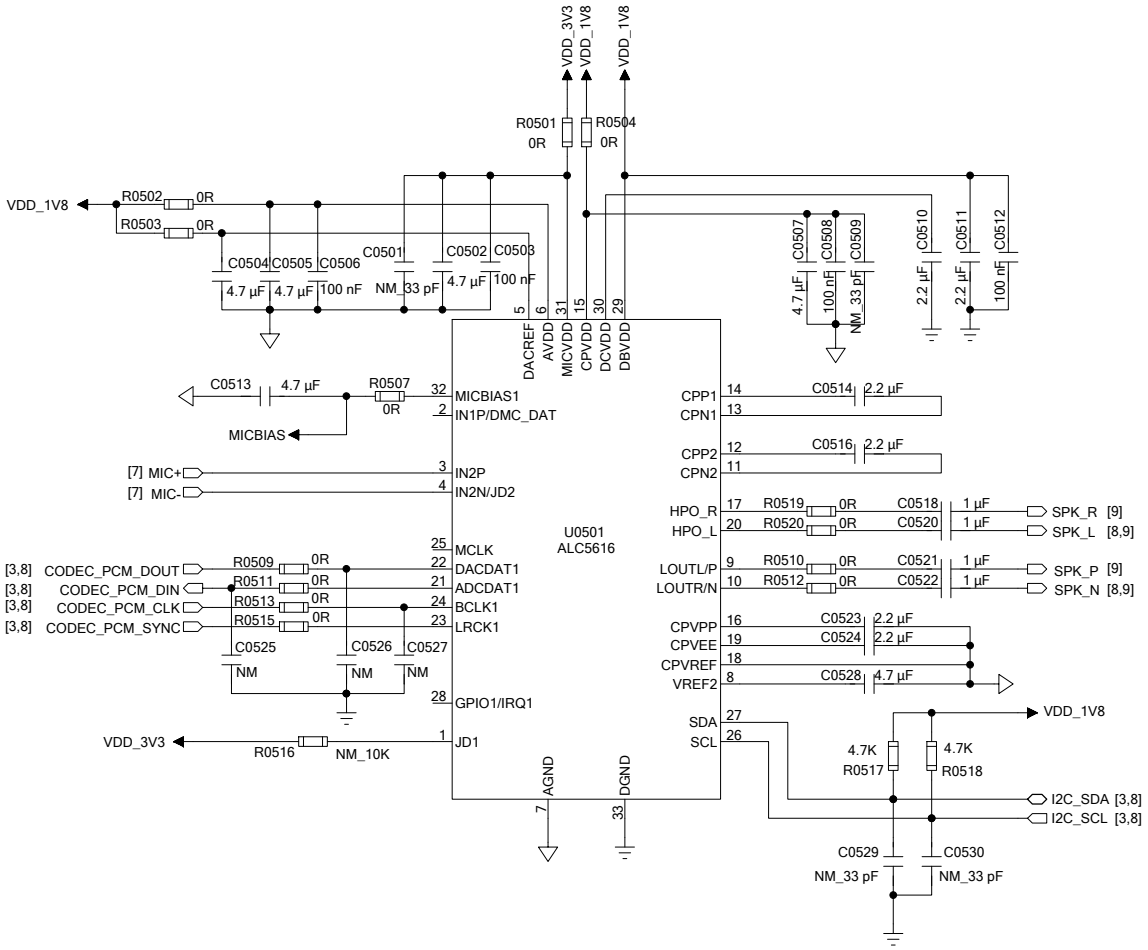
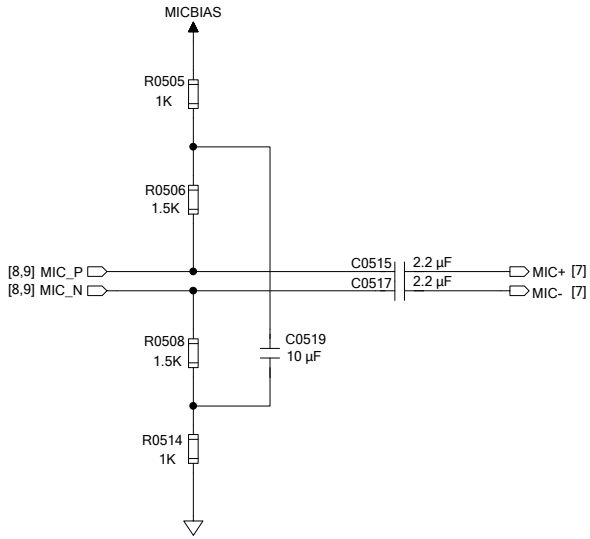
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 6 OF 14	DATE 2020/7/16

Audio Codec Design (ALC5616)





Notes:

1. ALC5616 power-on sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD -> MICVDD -> software initialization.
2. ALC5616 power-off sequence: disable codec function by software-> MICVDD -> DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. Module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be powered on before that.
4. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as 0805. For more details, please refer to Sheet “Audio Codec Design (Analog Interfaces)”.

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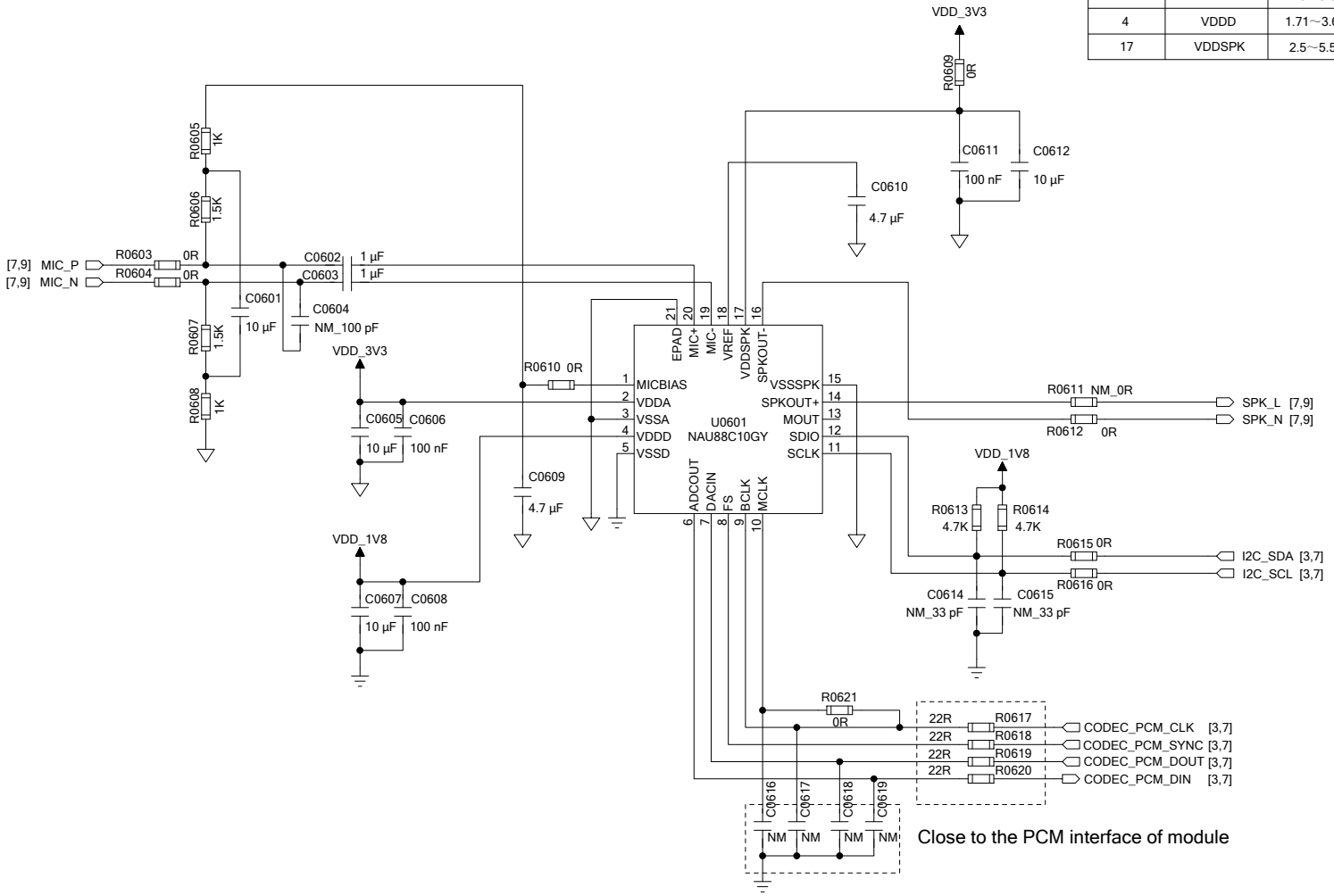
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 7 OF 14	DATE 2020/7/16

Audio Codec Design (NAU88C10GY)

Pin No.	Pin Name	Voltage	Description
2	VDDA	2.5~3.6 V	Analog VDD
4	VDDD	1.71~3.6 V	Digital VDD
17	VDDSPK	2.5~5.5 V	Speaker power supply



Notes:

1. The codec part should be away from interference sources such as RF and power supply, and the codec audio signal should surrounded with ground as much as possible.
2. The voltage of VDDA pin must always be no lower than that of VDDD.
3. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as 0805. For more details, please refer to Sheet “Audio Codec Design (Analog Interfaces)”.

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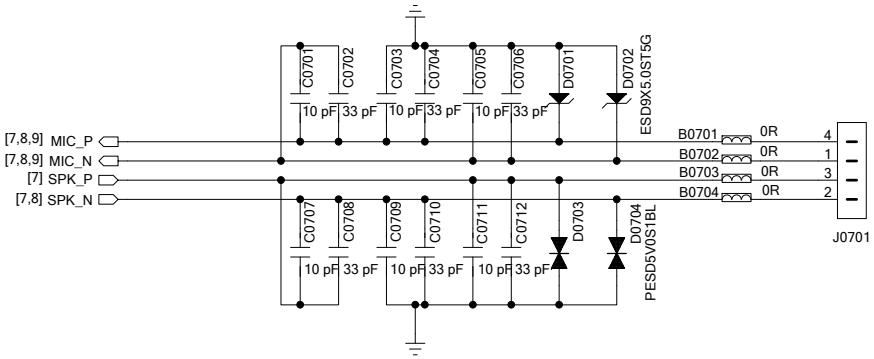
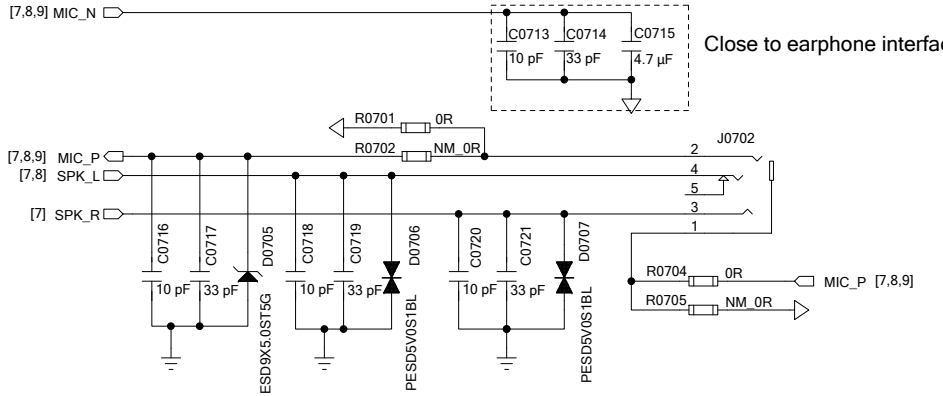
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 8 OF 14	DATE 2020/7/16

Audio Codec Design (Analog Interfaces)

Handset Application



Earphone Application



	CTIA	OMTP
R0702/R0705	NM	M
R0701/R0704	M	NM

Notes:

1. The analog output only drives earphone and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.
2. In handset application, both the MIC and SPK signal traces need to be routed as differential pairs.
3. In earphone application, the MIC signal traces need to be routed as differential pairs.
4. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises such as clock and DC-DC signals, etc.
5. ALC5616 and NAU88C10GY cannot be used simultaneously in audio codec design.

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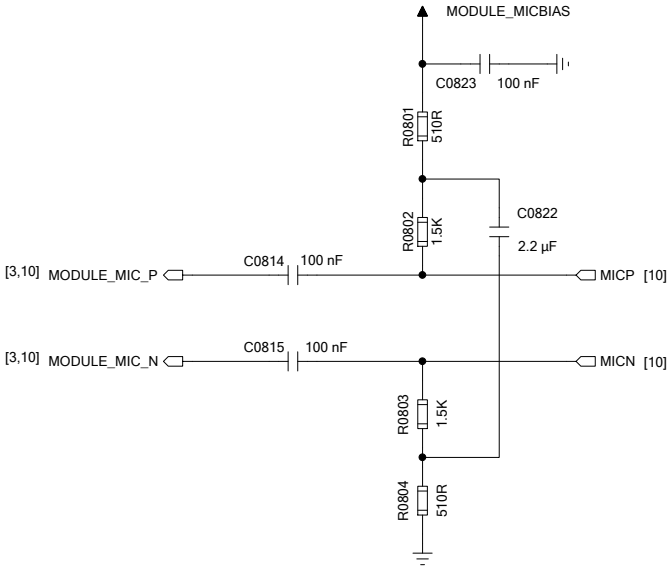
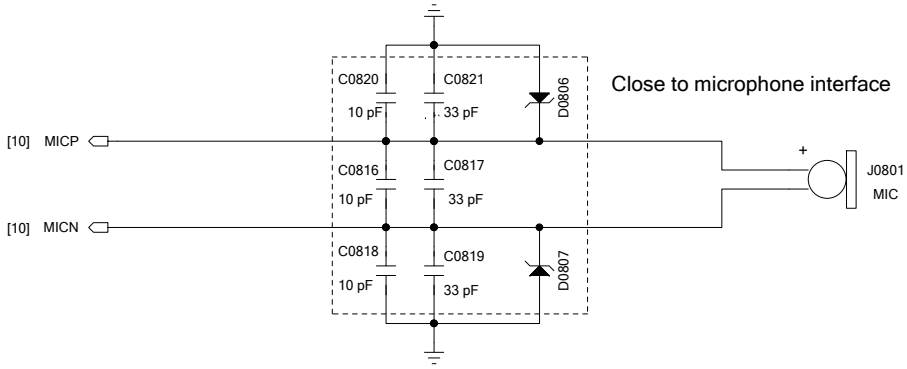
	SHEET 9 OF 14	DATE 2020/7/16

Module Analog Audio Design

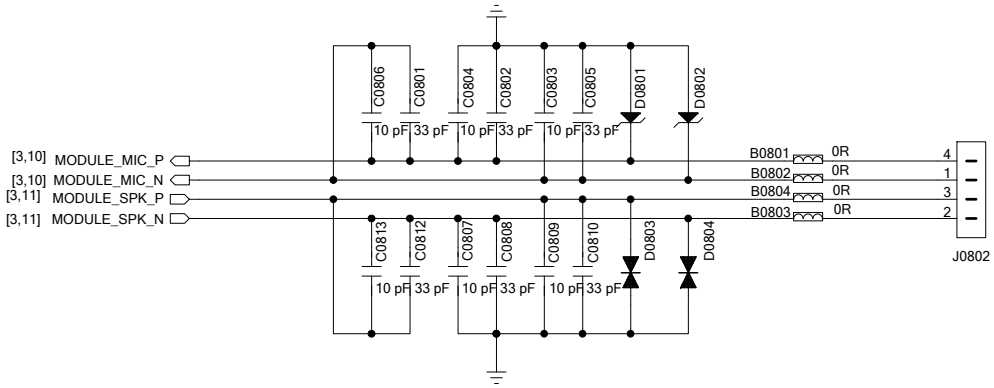
Microphone Bias Circuit



Microphone Application



Handset Application



Notes:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises.
3. In the audio design, the analog audio of the module and codec can be selected with only one or both, but it is not necessary to select both.
4. The analog output only drives handset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.

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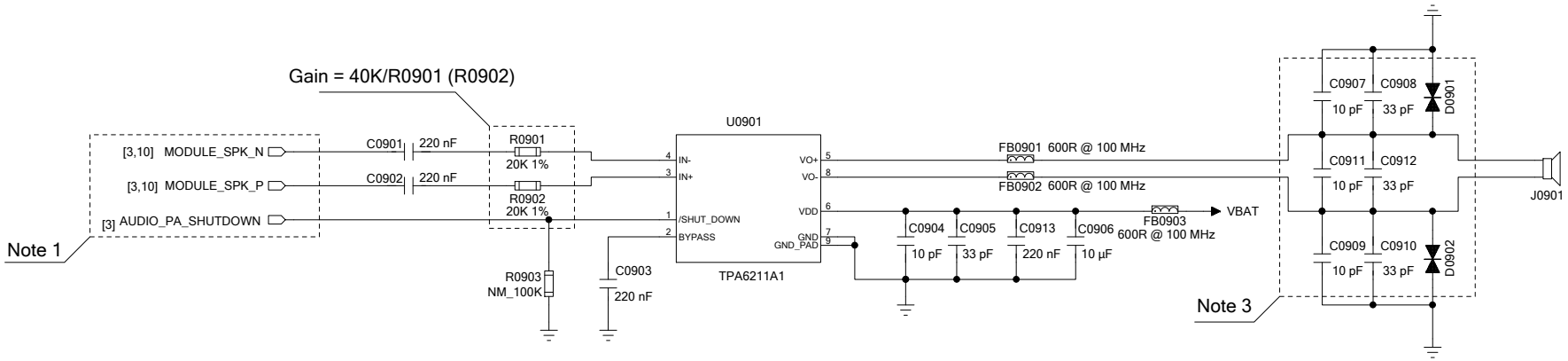
DRAWN BY Vane WANG	PROJECT EC200S-CN	TITLE Reference Design
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 10 OF 14	DATE 2020/7/16

Module Analog Audio Design (Audio Power Amplifier)



Notes:

1. SPK_P and SPK_N are differential outputs. It is recommended to use pin 116 of the module to control the enable pin of the audio power amplifier to eliminate POP.
   For detailed information of the pin, please contact Quectel Techinical Supports.
2. Select the audio power amplifier of appropriate power according to actual needs.
3. Place filter capacitors and ESD protection components close to the speaker.

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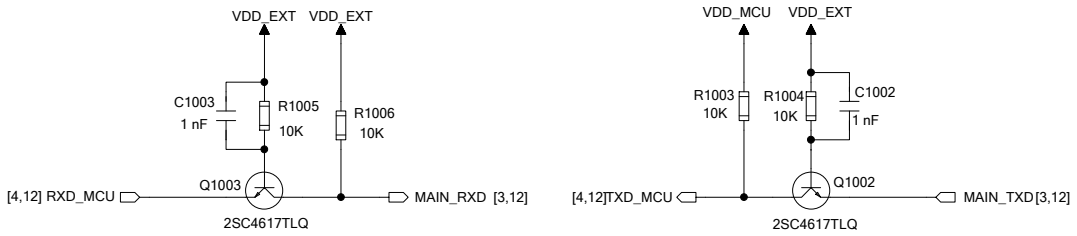
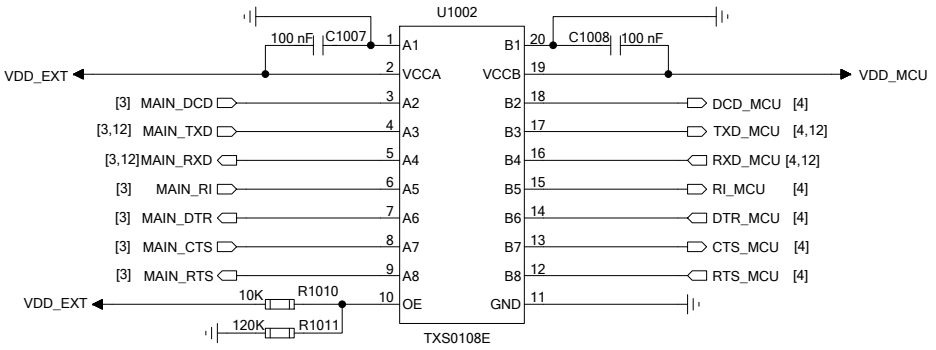
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 11OF 14	DATE 2020/7/16

UART Interfaces Design

UART Translation - Transistor Solution



UART Translation - IC Solution



Notes:

1. There are two translation solutions: transistor solution and IC solution, and it is recommended to select the latter.
2. The power supply of TXS0108E's VCCA should not exceed that of VCCB. For more information, please refer to the datasheet from TI.
3. The transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C1002 and C1003 of 1 nF can improve the signal quality.
4. The RTS and DTR transistor circuits are similar to that of the RXD interface. The CTS, RI and DCD transistor circuits are similar to that of the TXD interface.

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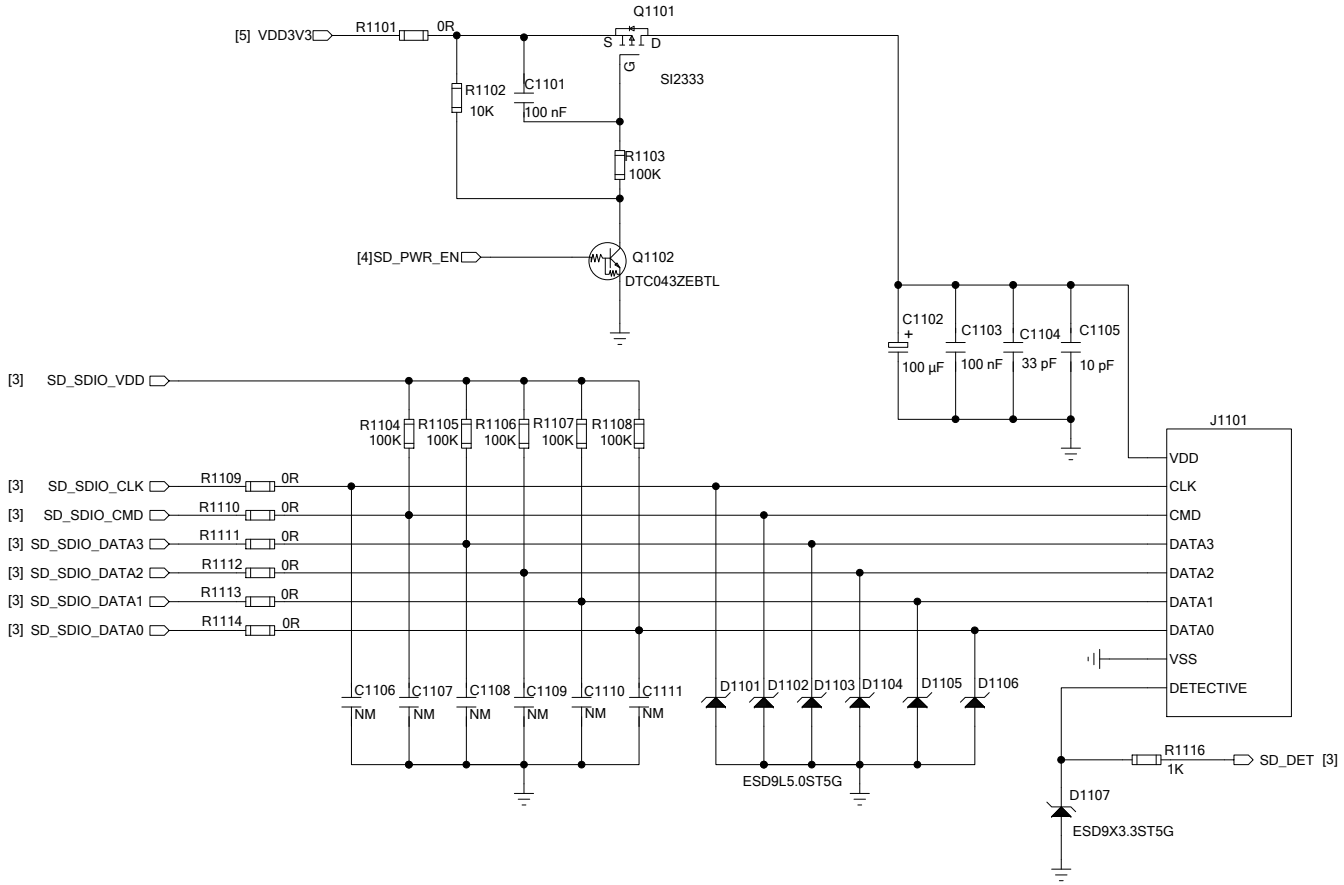
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 12 OF 14	DATE 2020/7/16

SD Card Interface Design



Notes:

1. The pin 34 (SD_SDIO_VDD) on the module can only be used for the pull-up resistor of SDIO bus and its maximum output current is 50 mA.
2. The supply voltage range of VDD for SD card is 2.7-3.6 V and needs to be provided with sufficient current up to 0.8 A.
3. To avoid the jitter of bus, pull-up resistors R1104-R1108 are recommended to be added to SDIO bus. SD_SDIO_VDD should be used as the pull-up power. The values of these resistors are among 10-100 kΩ and the recommended value is 100 kΩ.
4. In order to adjust the signal quality, it is recommended to add 0 Ω resistors R1109-R1114 in series between the module and the SD card connector. The bypass capacitors C1106-C1111 are reserved and not mounted by default.
5. It is recommended to add ESD protection components near the pins of SD card connector. The parasitic capacitance of ESD protection components should be smaller than 15 pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock and DC-DC signals, etc.
7. Route SDIO signals with 50 Ω ±10% impedance. It is important to route SDIO signals surrounded with ground on the layer and ground planes above and below, and the total trace length should be less than 50 mm.
8. It is recommended to keep the trace length difference among SD_SDIO_CLK and SD_SDIO_DATA[0:3]/SD_SDIO_CMD less than 1 mm.
9. Make sure the adjacent trace spacing is two times the trace width and the bus capacitance is less than 15 pF.

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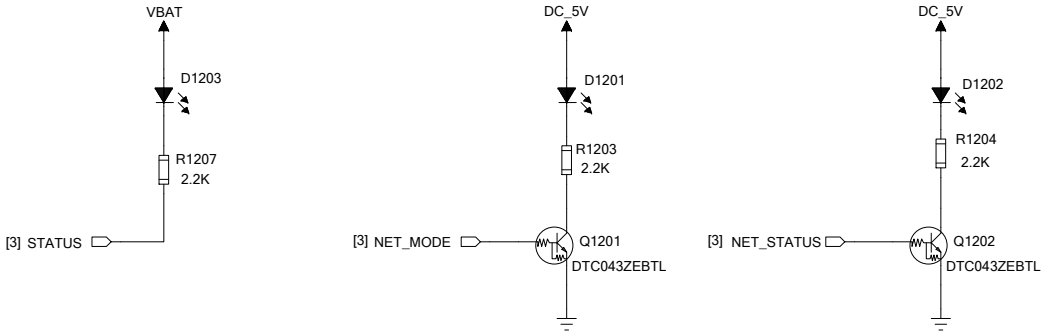
DRAWN BY Vane WANG	PROJECT EC200S-CN	TITLE Reference Design
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 13 OF 14	DATE 2020/7/16

Other Designs

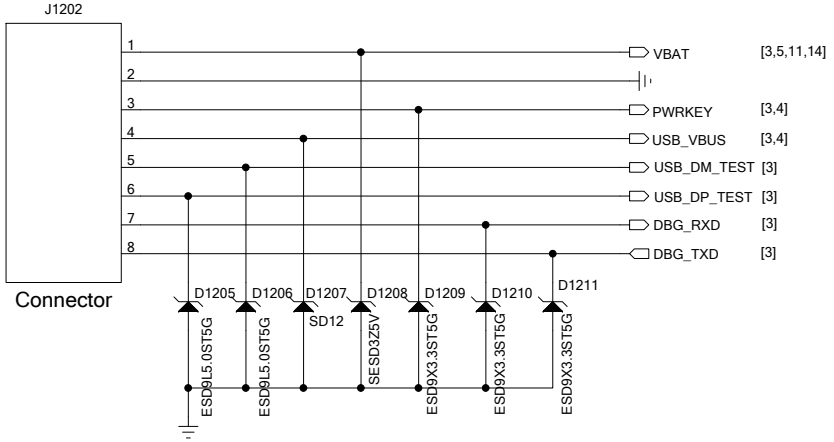
Indicators



Notes:

1. The STATUS is an open drain output pin.
2. For more details about NET_MODE and NET_STATUS, please refer to *Quectel_EC200S-CN_Hardware_Design.*
3. If the low current consumption is required when the customers' device is in sleep, replace the power supply VBAT and DC_5V of the STATUS, NET_MODE, NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

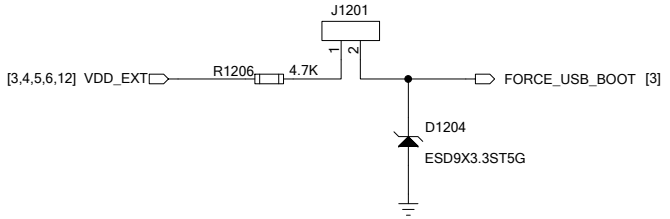
Reserved Test Points



Notes:

1. Test points for both USB and debug UART interfaces are reserved for catching logs.
2. Test points for USB interface also can be reserved for firmware upgrade.
3. The junction capacitance of the ESD protection componets on USB data lines should be less than 2 pF.
4. The debug UART interface supports 1.8 V power domain, and a level translator should be used if the power domain of customers' application is 3.3 V.

Emergency Download



Notes:

1. It is recommended to reserve the FORCE_USB_BOOT interface design.
2. FORCE_USB_BOOT is kept open by default.
   When it is at a high level, the module will enter download mode.

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DRAWN BY Vane WANG	PROJECT EC200S-CN	TITLE Reference Design
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 14 OF 14	DATE 2020/7/16